NOVATEK
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Data Sheet

NT50805

TFT-LCD Multi-Channel DC-DC Converters

V0.0

History

Version	Content	Page	Date
0.0	New SPEC	All	2022/9/6

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General Description

The NT50805 includes 2-wire I2C interface, one synchronous boost converter for positive-voltage AVDD supply, one synchronous inverting converter for negative-voltage AVEE supply, two high-performance buck converters, one low dropout linear regulator (LDO), one SIBO (Single Inductor Bipolar Output) switching converter for VGH supply and VGL supply, two programmable voltage buffers for gamma voltages and a programmable voltage buffer for VCOM.

The synchronous boost converter and the synchronous inverting converter provide the regulated supply voltage for the panel source driver ICs. The synchronous boost converter is a high-frequency (programmable) current-mode regulator with an integrated 16V N-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors.

Two buck converters provide the regulated supply voltage for core power of T-con, and digital power of source driver ICs. The buck converter is a high-frequency current-mode regulator with an integrated N/P-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors. In addition, one low dropout linear regulator provides the supply voltage for I/O interface power.

NT50805 includes SIBO converter provides a pair of the positive VGH voltage (TFT gate-on supply) and the negative VGL voltage (TFT gate-off supply) for gate driver ICs or level shifter IC. The burst mode of SIBO converter can enhance the light load efficiency.

NT50805 also includes a voltage detector to monitoring the input supply voltage to issue a reset signal while the detected voltage is lower than a programmable threshold voltage. The VCOM buffer can drive the LCD backplane VCOM, which can be a positive or a negative VCOM output. In addition, two gamma buffers can provide the gamma reference voltages of source driver ICs.

NT50805 has current-limit function for the internal switches of the converters, and the shutdown protection for output fault condition of the converters/regulator. Programmable soft-start function is also built-in to limit the start-up inrush current.

NT50805 is available in a 28-pin thin FCQFN 3.5x3.5 package with a typical thickness of 0.8mm for ultra-thin LCD panels.

Features

- 2.5V to 5.0V Input Supply Range
- 2-wire I2C interface
  Programmable Power Sequence Control Programmable Voltages Supply
- Synchronous Boost Converter for AVDD
  Built-In N/P-Channel MOSFET with Diode-Free
  For Positive Voltage Supply of Source-IC
  Driving ability 400mA
  Over-Current Protection
- Synchronous Inverting Converter for AVEE
  For Negative Voltage Supply of Source-IC
  Driving ability 400mA
- Two Current-Mode Buck Converters for VCORE and VIO
  Built-In P/N-Channel MOSFET with diode free
- SIBO Converter for VGH and VGL
  Built-In N/P-Channel MOSFET
- Low Voltage Detector
- Programmable Positive/Negative VCOM voltage buffer
  ±150mA Output Short-Circuit Current
- Two Programmable Gamma voltage buffers
  ±10mA Output Short-Circuit Current
- Over Temperature Protection
- Over-Current Protection of Converters
- Under-Voltage Protection of Converters/Regulator
- Software and Hardware UBRR Function Control
- Support two device address select
- FCQFN-28L 3.5x3.5 Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

TFT-LCD Tablets
GIP/Non-GIP Notebook Displays

Ordering Information

Part No.	Package	Marking
NT50805PG-028/A	FCQFN-28 3.5x3.5	50805

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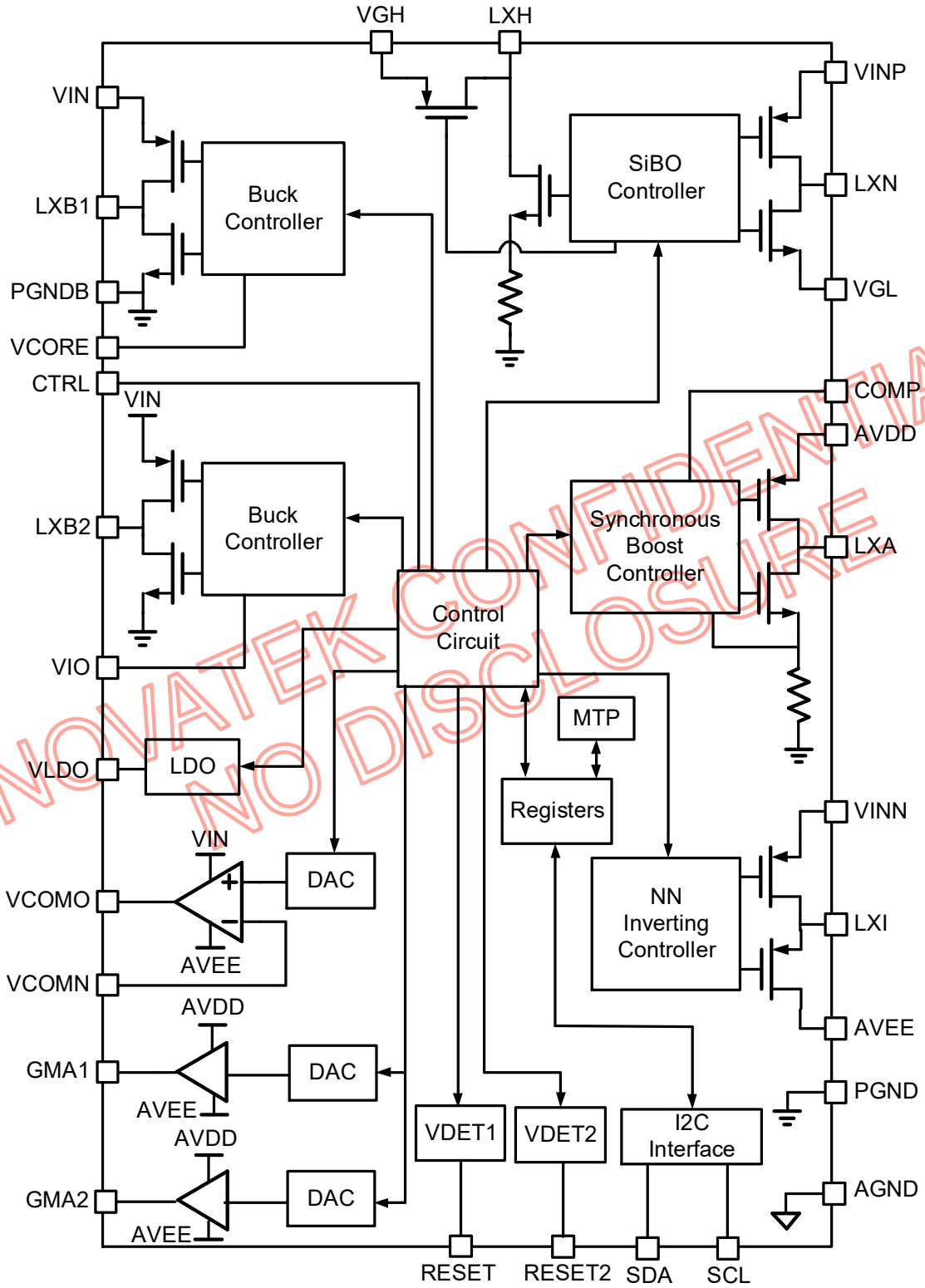
Function Diagram



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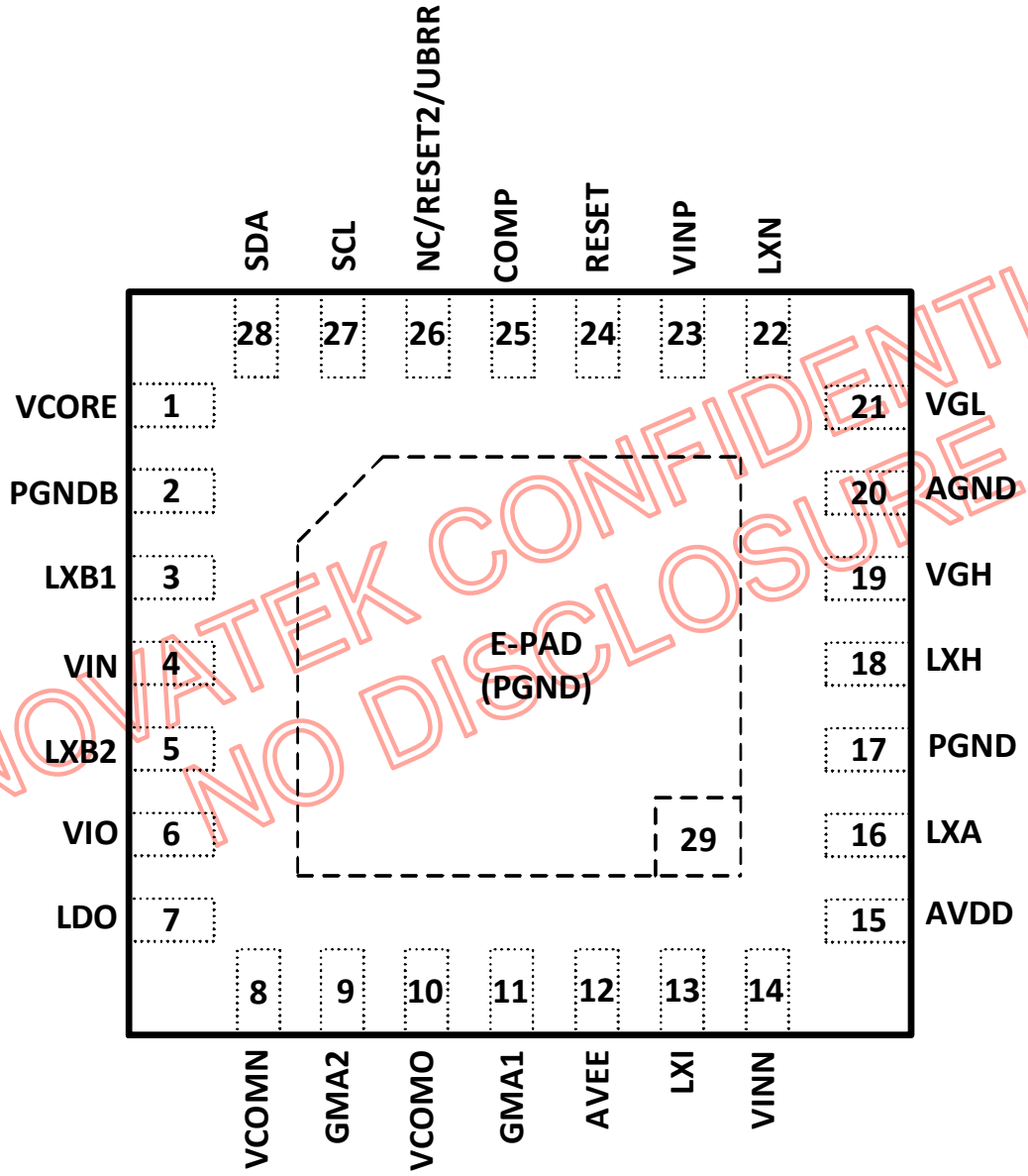
Pin Configuration

(Top view - Perspective)



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Pin Description

PIN	Name	Type	Function
1	VCORE	I	Input Voltage of VCORE Buck Converter to Regulate Output Voltage.
2	PGNDB	P	Power Ground of Buck Converters.
3	LXB1	P	Switching Pin. Drain of Internal Power NMOS for VCORE Buck Converter.
4	VIN	P	Power Supply Input of IC
5	LXB2	P	Switching Pin. Drain of Internal Power NMOS for VIO Buck Converter.
6	VIO	I	Input Voltage of VIO Buck Converter to Regulate Output Voltage.
7	LDO	O	LDO Output.
8	VCOMN	I	Inverted-terminal of VCOM Buffer
9	GMA2	O	Negative GMA2 Buffer Output.
10	VCOMO	O	VCOM Buffer Output.
11	GMA1	O	Positive GMA1 Buffer Output.
12	AVEE	O	Negative AVEE Voltage Output for Source-IC.
13	LXI	P	Switching Pin. Drain of Internal Inverter Converter.
14	VINN	P	Power Supply Input of AVEE Inverting Converter.
15	AVDD	O	Positive AVDD Voltage Output for Source-IC.
16	LXA	P	Switching Pin of AVDD Boost Converter.
17	PGND	P	Power Ground of AVDD Boost Converter and SIBO Converter.
18	LXH	P	VGH Switching Pin of SIBO Converter.
19	VGH	O	TFT Gate-ON Voltage Output of VGH.
20	AGND	P	Analog Ground.
21	VGL	O	TFT Gate-Off Voltage Output of VGL.
22	LXN	P	VGL Switching Pin of SIBO Converter.
23	VINP	P	Power Supply Input of SIBO Converter
24	RESET	O	Output Pin of Low Voltage Detect.
25	COMP	O	Compensation Pin of AVDD Boost Converter.
26	NC	-	Floating this pin. Do not connect to any other pins or circuit.
	RESET2	I	Output Pin of Low Voltage Detect.
	UBRR	I	UBRR Control pin Pull to GND with 100kohm internally.
27	SCL	I	2-Wire I2C Interface Clock Input.
28	SDA	I/O	2-Wire I2C Interface Data Input.
29	E-pad	P	Power Ground. (PGND) The exposed pad must be soldered to a large PCB and connected to GND for heat dissipation.

Note: P: power/ground; I: Input; O: Output; I/O: Bi-direction

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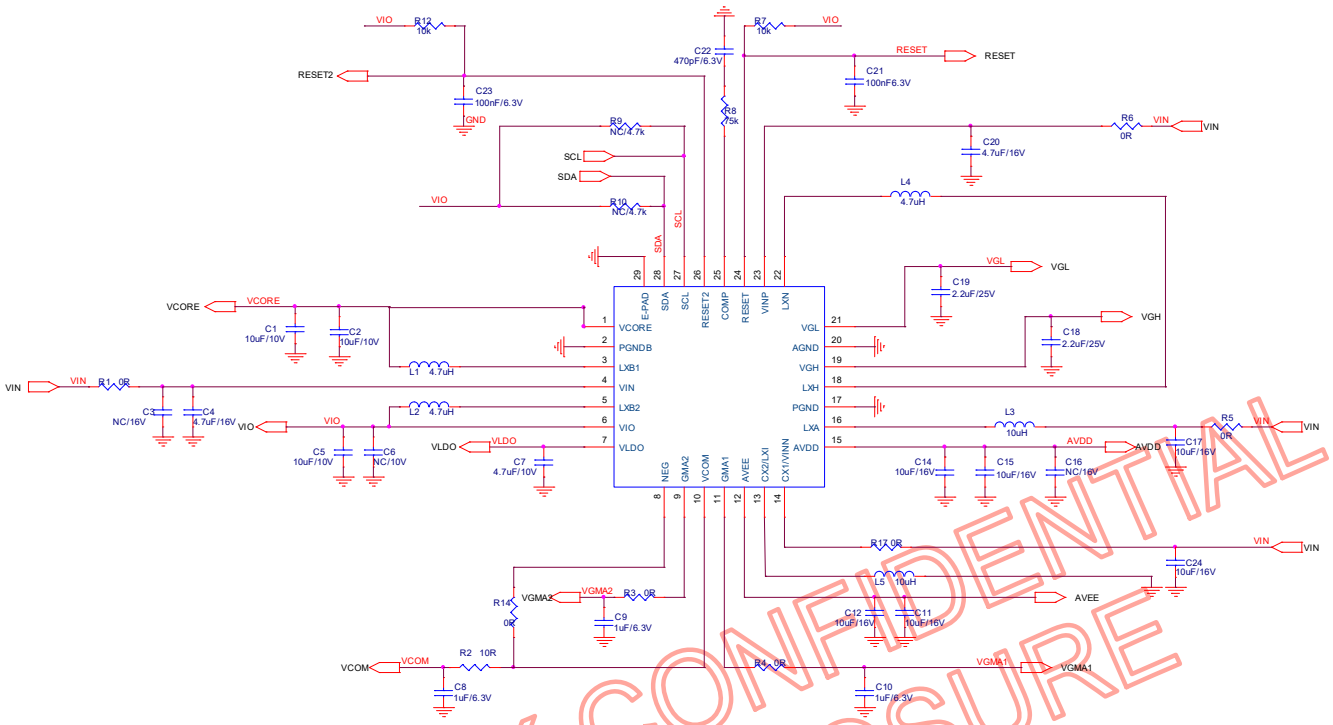
Application Circuit for Pin26=RESET2 (FCQFN3.5x3.5)



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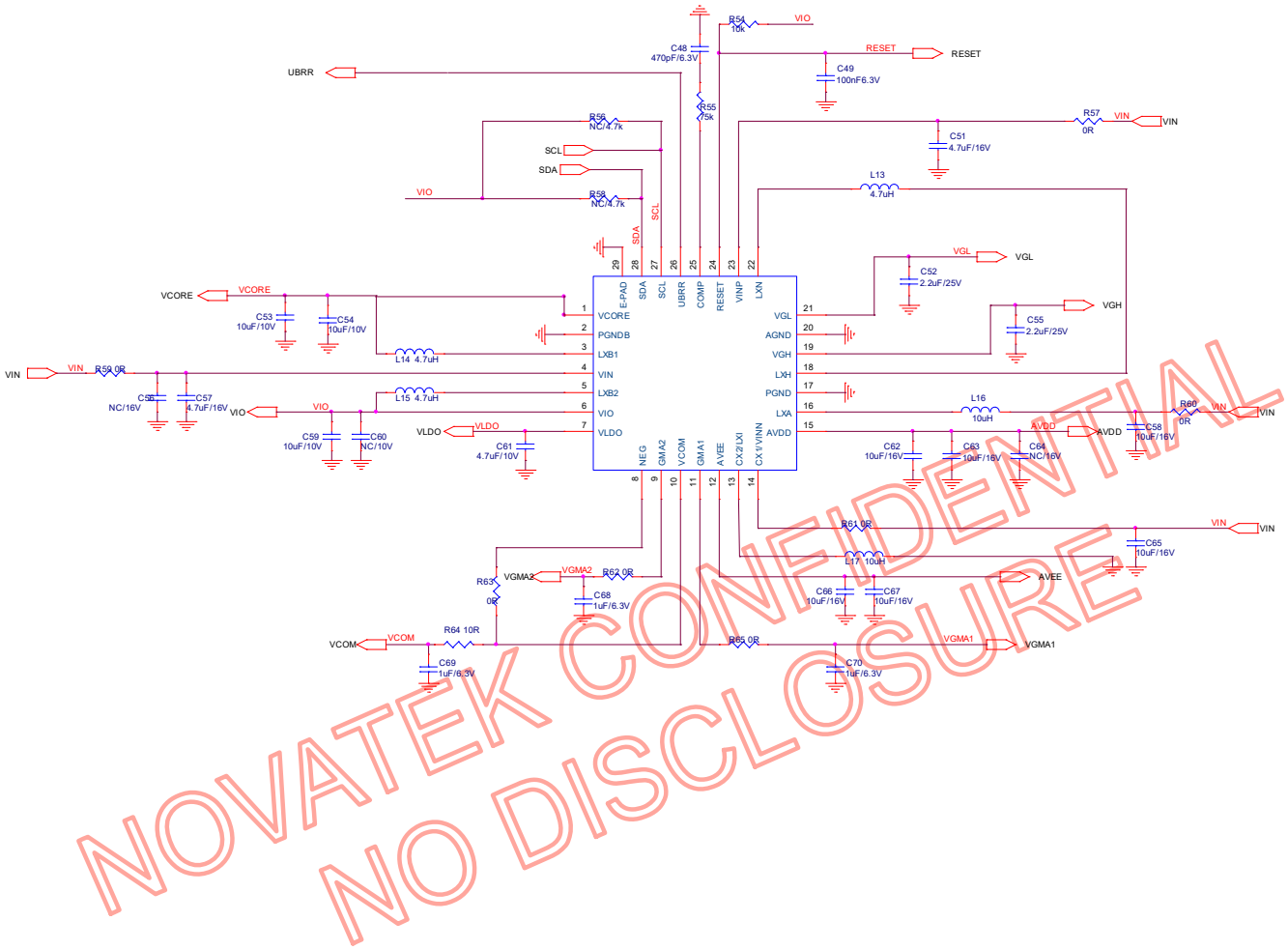
Application Circuit for Pin 26=UBRR (FCQFN3.5x3.5)



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Absolute Maximum Ratings

VIN, VINP, VINN, SDA, SCL to AGND.....-0.3V to +10V
RESET, RESET2, COMP to AGND.....-0.3V to +6.0V
LDO, VCORE, VIO to AGND..... -0.3V to +6.0V
LXB1 and LXB2 to PGNDB..... -0.3V to +6.0V
AVDD, LXA, GMA1 to PGND..... -0.3V to +7.0V
AVEE to PGND..... -0.3V to -7.0V
LXI to PGND ..... -7.0V to +6.0V
VGH, LXH to PGND..... -0.3V to +30V
VGL, LXN to PGND..... 0.3V to -20V
VCOMN, VCOM to PGND ..... -7 V to +10 V
GMA2 to PGND ..... -7 V to +7 V
PGND, PGNDB to AGND ..... ±0.3V
VIN / SDA / SCL / VINP / VINN to GND (100ms pulse) .....-0.3V to +10V

Junction Temperature .....+125°C
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range .....-40°C to +150°C
ESD Susceptibility (HBM) 3KV
SDA / SCL ESD Gun.....±8kV
ESD Susceptibility (CDM) 750V

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN}＝V_{INN}＝3.3V, AVDD =6V, AVEE= -6V, VGH=18V, VGL=-14V, PGND＝AGND＝0V. Typical values are at T_A＝25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
VIN Supply Range	V_{IN}		2.5	–	5.0	V
VINN Supply Range	V_{INN}		2.5	–	5.0	V
VINP Supply Range	V_{INP}	When SIBO_ENH=0	2.5	–	5.0	V
		When SIBO_ENH=1	5.0		7.0	V
VIN Quiescent Current	I_{VIN}		–	–	5	mA
VIN Quiescent Current	I_{VIN}	All block disable			1	mA
VIN Under-Voltage Lockout Threshold	V_{UVLO}	VIN rising	2.3	2.4	2.5	V
		Hysteresis	–	0.5	–	
Over Temperature Protection	T_{OTP}	Temperature rising	–	150	–	℃
		Hysteresis	–	20	–	
Current Mode Boost Converter – AVDD						
Operating Frequency	F_{SW_LXA}	600kHz/715kHz/800kHz/1000kHz/1225kHz	600	–	1225	kHz
Frequency Accuracy		F_{SW_LXA}=715kHz	95	100	105	%
		Others	90	100	110	%
Maximum Duty Cycle	D_{MAX_AVDD}		–	90	–	%
Under Voltage Protection	$V_{UVP\text{-}AVDD}$	V_{AVDD} falling under Target percentage	–	80	–	%
AVDD Fault Condition		UVP continued occur	–	60	–	ms
Output Voltage Range	V_{AVDD}	50mV/step	4.0	-	7.0	V
Output Voltage Accuracy	V_{ACC_AVDD}	no load	99	100	101	%
Output Load Regulation		V_{AVDO}=6.0V, I_{LOAD}＝10 to 400mA, F_{SW_LXA}=715kHz	–	75	–	mV/A
Output Line Regulation		V_{IN}=2.5V~5.0V	–	0.1	0.15	%/ V
Current Limit	I_{LIM_AVDD}	0.5A/1A/1.5A/2.0A	0.5	–	2	A
Output Current Capability		V_{AVDO}=6.0V	400	–	–	mA
Output Voltage -- AVEE						
Operating Frequency	F_{SW_LXI}	1* F_{SW_LXA}	–	F_{SW_LXA}	–	Hz
Frequency Accuracy		compare with target	90	100	110	%
Output Voltage	V_{AVEE}	100mV/step	-7.0	–	-4.0	V

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Output Voltage Accuracy	$V_{ACC-AVEE}$	no load	98.5	100	101.5	%
Under Voltage Protection	$V_{UVP-AVEE}$	V_{AVEE} falling under target	–	80	–	%
Fault Condition		UVP continued occur	–	60	–	ms
Output Load Regulation (Buck-Boost)		V_{AVEE}=-6V , I_{LOAD}＝10 to 400mA, F_{SW_LXA}=715kHz	–	200	–	mV/A
Output Line Regulation		V_{IN}=2.5V~5.0V	–	0.1	0.15	%/ V
Current Limit	I_{LIM_AVEE}	1.5A/2A/2.5A/3A	1.5	–	3	A
Output Current Capability		V_{AVEE}= -6V	400	–	–	mA
Current Mode Buck Converter 1 – V_{CORE}						
Operating Frequency	F_{SW_LXB1}	600kHz/715kHz/800kHz/1000kHz/1225kHz	600	–	1225	kHz
Frequency Accuracy		F_{SW_LXB1}=715kHz	95	100	105	%
		Others	90	100	110	%
VCORE Output Voltage	V_{CORE}	20mV/step	0.8	–	2.06	V
Output Voltage Accuracy	$V_{ACC-VCORE}$	no load	99	100	101	%
Under Voltage Protection	$V_{UVP-VCORE}$	V_{CORE} falling under target	–	80	–	%
VCORE Fault Condition		UVP continued occur	–	60	–	ms
Output Load Regulation		V_{CORE}=1.2V,I_{LOAD}＝10 to 700mA	–	50	–	mV/A
Output Line Regulation		V_{IN}＝2.5V to 5.0V	–	0.1	0.15	%/ V
LXB1 Current Limit	I_{CORE_LIM}		–	1.5	–	A
Maximum Driving Ability		V_{IN}=3.3V, V_{CORE}=1.2V , F_{SW_LXB1}=1225kHz	850	–	–	mA
Current Mode Buck Converter 2 – V_{IO}						
Operating Frequency	F_{SW_LXB2}	600kHz/715kHz/800kHz/1000kHz/1225kHz	600	–	1225	kHz
Frequency Accuracy		F_{SW_LXB2}=715kHz	95	100	105	%
		Others	90	100	110	%
VIO Output Voltage	V_{IO}	50mV/step	1.0	–	2.55	V
Output Voltage Accuracy	$V_{ACC-VIO}$	no load	99	100	101	%
Under Voltage Protection	$V_{UVP-VIO}$	V_{IO} falling under target	–	80	–	%
VBUCK1 Fault Condition		UVP continued occur	–	60	–	ms
Output Load Regulation		V_{IO}=1.8V, I_{LOAD}＝10 to 400mA	–	50	–	mV/A
Output Line Regulation		V_{IN}＝2.5V to 5.0V	-	0.1	0.15	%/ V
LXB2 Current Limit	I_{IO_LIM}		–	1.3	–	A
Maximum Driving Ability		V_{IN}=3.3V, V_{IO}=1.8V, F_{SW_LXB2}=1225kHz	400	–	–	mA
Low Drop Output Regulator – V_{LDO}						
LDO2 Output Voltage	V_{LDO}	100mV/step	1.7	–	2.8	V
Output Voltage Accuracy	$V_{ACC-LDO2}$	no load	99	100	101	%
Output Load Regulation		I_{LOAD}＝1 to 100mA	-1	–	1	%
Output Line Regulation		V_{IN}＝2.5V to 5.0V, I_{LOAD}=10mA	–	0.1	0.15	%/ V
Output Current Capability		V_{IN}＝2.5V to 5.0V, I_{LOAD}=10mA	100	–	–	mA
Dropout voltage		V_{IN}＝2.8V, V_{LDO}=2.8V, I_{LOAD}=100mA		0.2		V
SIBO Converter – V_{GH}						
Operating Frequency	F_{SW_LXH}	SIBO_FREQH=0，500kHz/600kHz/715kHz/800kHz/913kHz/1000kHz/1225kHz	500	–	1225	kHz
	F_{sw_LXH}	SIBO_FREQH=1，1/2* F_{SW_LXH}	250		612.5	kHz
Frequency Accuracy		F_{SW_LXH}=715kHz	95	100	105	%
		Others	90	100	110	%

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Output Voltage Range	V_{VGH}	200mV/step, VGH_High Resolution=0	6.0	–	12	V
Output Voltage Range	V_{GH}	500mV/step, VGH_High Resolution=1	12.5	–	30	V
Output Voltage Accuracy	$V_{acc\text{-}VGH}$	no load	97	100	103	%
Under Voltage Protection	$V_{UVP\text{-}VGH}$	V_{VGH} falling under Target percentage	–	80	–	%
VGH Fault Condition		UVP continued occur	–	60	–	ms
Current Limit	I_{LIM_LXH}		–	1	–	A
Maximum Driving Ability		V_{INP} =3.3V，VGH=18V, F_{SW_LXH}=715kHz	5	–	–	mA
		V_{INP} =6V，VGH=18V, F_{SW_LXH}=715kHz	25	–	–	mA
SIBO Converter – V_{GL}						
Operating Frequency	F_{SW_LXN}	SIBO_FREQH=1，500kHz/600kHz/715kHz/800kHz/913kHz/1000kHz/1225kHz	500	–	1225	kHz
	F_{sw_LXN}	SIBO_FREQH=1，1/2* F_{SW_LXN}	250		612.5	kHz
Frequency Accuracy		F_{SW_LXN}=715kHz	95	100	105	%
		Others	90	100	110	%
Output Voltage Range	V_{GL}	0.2V/step	-18	–	-5.4	V
Output Voltage Accuracy	$V_{acc\text{-}VGL}$	no load	97	100	103	%
Under Voltage Protection	$V_{UVP\text{-}VGL}$	V_{VGL} rising under Target percentage	–	80	–	%
VGL Fault Condition		UVP continued occur	–	60		ms
Current Limit	I_{LIM_LXN}		–	1	–	A
Maximum Driving Ability		V_{INP} =3.3V，V_{GL} =-14V, F_{SW_LXH}=715kHz	5	–	–	mA
		V_{INP} =6V，V_{GL} =-14V, F_{SW_LXH}=715kHz	25	–	–	mA
Voltage Detector – RESET						
Detection Voltage	V_{RESET}	100mV/step	2	–	2.7	V
Detecting Voltage Accuracy	$V_{acc\text{-}RESET}$	No load	98	100	102	%
Voltage Detector – RESET2						
Detection Voltage	V_{RESET2}	100mV/step	2	–	2.7	V
Detecting Voltage Accuracy	$V_{acc\text{-}RESET2}$	No load	98	100	102	%
Programmable VCOM and output buffer – V_{COM}						
VCOM Output Voltage	V_{COM}	0.01V/step	-3.6	–	2.02	V
Output Voltage Accuracy	$V_{acc\text{-}VCOM}$	No load	-10	–	10	mV
Output Voltage Ability		each step, I_{OUT}＝+/-10mA	–	15	–	mV
Short-Circuit Current		each step, maximum source/sink current	–	150	–	mA
Programmable gamma voltage and output buffer – V_{GMA1} and V_{GMA2}						
GMA1 Output Voltage	V_{GMA1}	0.02V/step	AVDD-1.26	–	AVDD	V
GMA2 Output Voltage	V_{GMA2}	0.02V/step	AVEE	–	AVEE+1.26	-
Output Voltage accuracy	$V_{acc\text{-}GMA}$	No load	-20	–	20	mV
Sort-Circuit Current			–	10	–	mA
UBRR PIN						
threshold voltage	VIH		1.2	–	–	V
	VIL		–	–	0.6	
I2C INTERFACE						
High Level Input Voltage	V_{IH}	VIN=2.5V to 5.0V	1.2	–	–	V
Low Level Input Voltage	V_{IL}	VIN=2.5V to 5.0V	–	–	0.6	V
EEPROM Write Time	T_{WRITE}		–	–	1.8	sec

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Number of Guaranteed EEPROM Write Cycles	N_{WRITE}		–	–	100	Cycles

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AC CHARACTERISTICS

Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
F_{SCL}	Clock Frequency, SCL	0	-	1000	kHz	
t_{LOW}	Clock Pulse Width Low	0.5	-		us	
t_{HIGH}	Clock Pulse Width High	0.26	-		us	
t_{BUF}	Time the bus must be free before a new transmission can start(2)	0.5			us	
$t_{HD.STA}$	Start Hold Time	0.26			us	
$t_{SU.STA}$	Start Setup Time	0.26			us	
$t_{HD.DAT}$	Data In Hold Time	0		900	ns	
$t_{SU.DAT}$	Data In Setup Time	100			ns	
t_R	Inputs Rise Time(2)			300	ns	
t_F	Inputs Fall Time(2)			300	ns	
$t_{SU.STO}$	Stop Setup Time	0.26			us	
t_{DH}	Data Out Hold Time	50		100	ns	
C_B	Bus Capacitance		5		pF	

Note: 2. This parameter is characterized and is not 100% tested.

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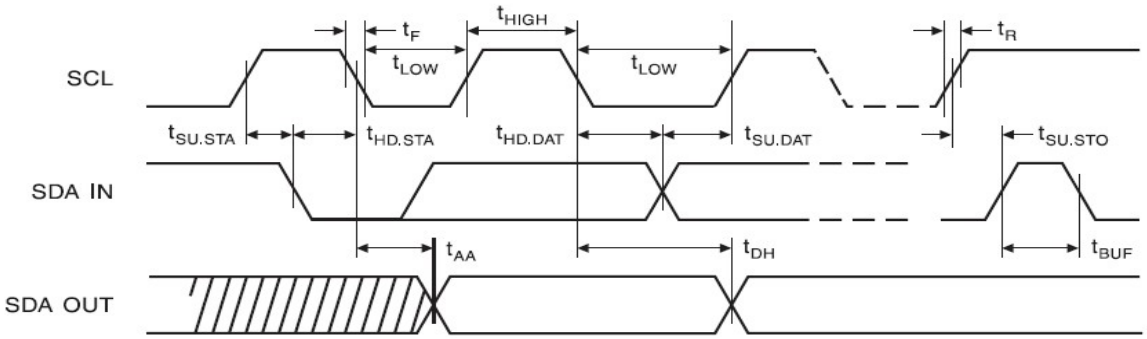
I2C Bus Timing :



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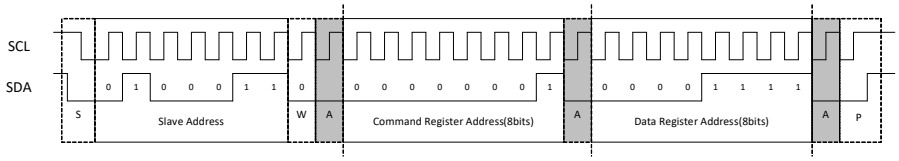
I2C Protocol for PMIC(版本1. No Write protect)

For A0 bit = 0

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
Slave address (23h, 7-bit) Read=1/Write=0	0	1	0	0	0	1	1	R/W	46h (8-bit)

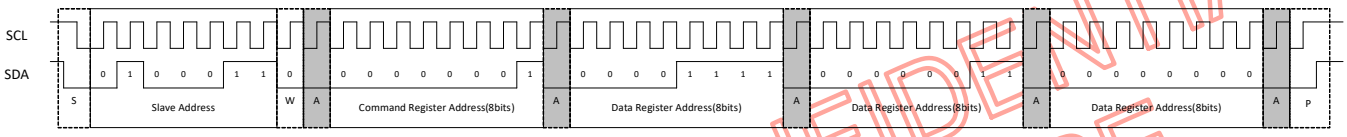
(a) Write Single Byte to DAC

Example: Write Data: 0Fh into DAC address 01h



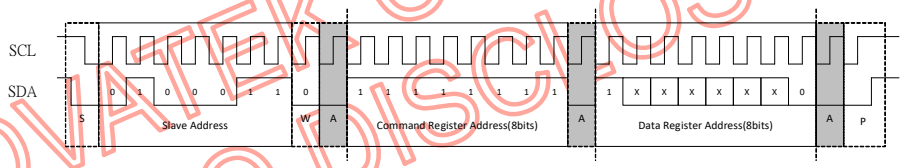
(b) Write Multiple Bytes to DAC

Example: Write Data: 0Fh, 03h, 00h into DAC address 01h, 02h, 03h…



(c) Write all DAC Registers to EEPROM

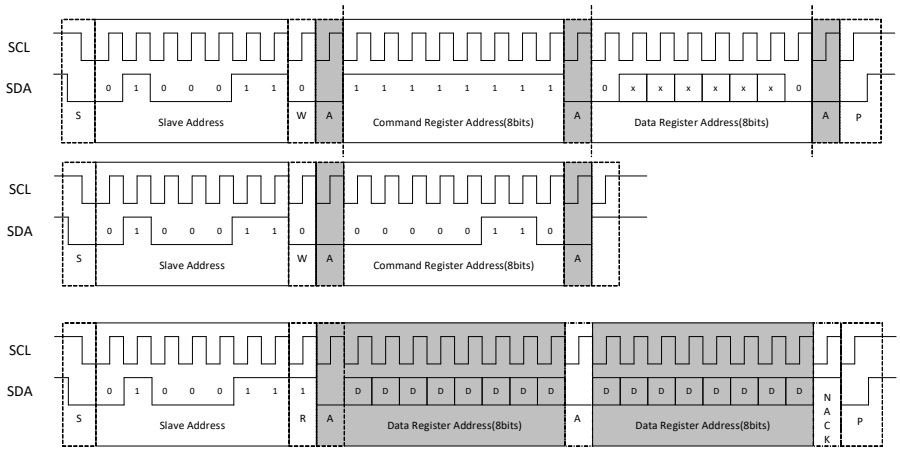
Example: Write Data: 80h into DAC address FFh



(d) Read Data from DAC

Example: Read data from DAC address 06h

Step 1: Command for reading DAC



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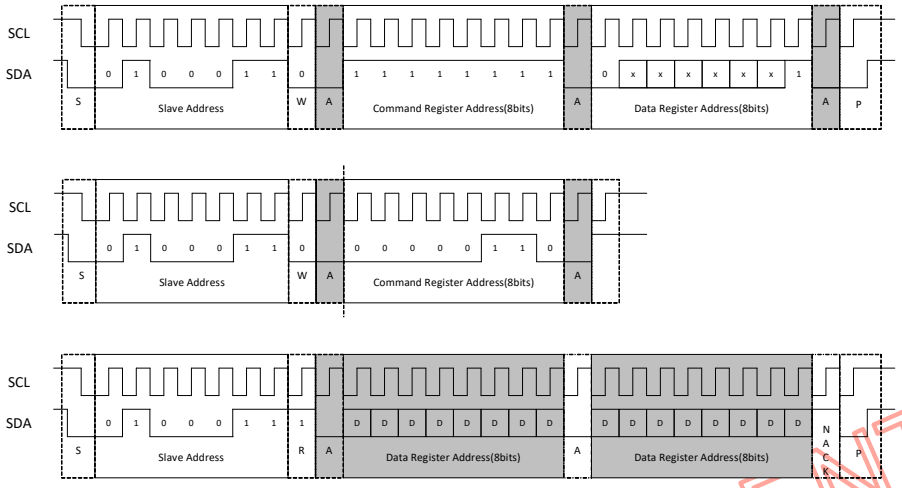
(e) Read Data from EEPROM

Example: Read data from EEPROM address 06h

Step 1: Command for reading EEPROM



From Master to Salve

From Slave to Master

Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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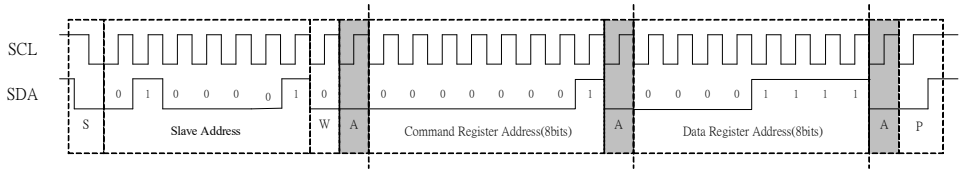
For A0 bit = 1

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
Slave address (21h, 7-bit) Read=1/Write=0	0	1	0	0	0	0	1	R/W	42h (8-bit)

(a) Write Single Byte to DAC

Example: Write Data: 0Fh into DAC address 01h

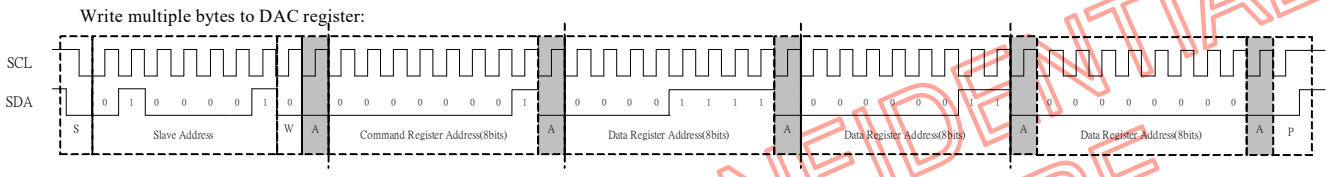
Write single byte to DAC register:



(b) Write Multiple Bytes to DAC

Example: Write Data: 0Fh, 03h, 00h into DAC address 01h, 02h, 03h…

Write multiple bytes to DAC register:



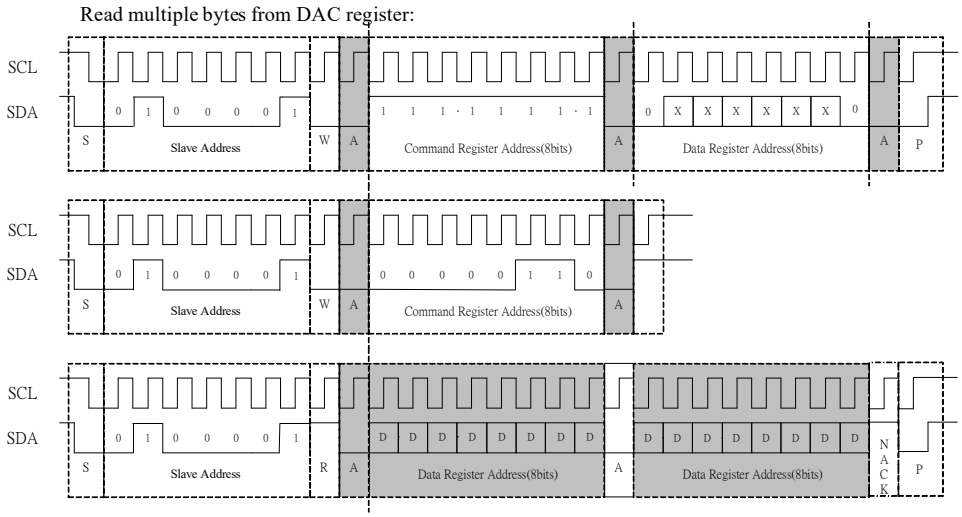
(c) Write all DAC Registers to EEPROM

Example: Write Data: 80h into DAC address FFh

(d) Read Data from DAC

Example: Read data from DAC address 06h

Read multiple bytes from DAC register:



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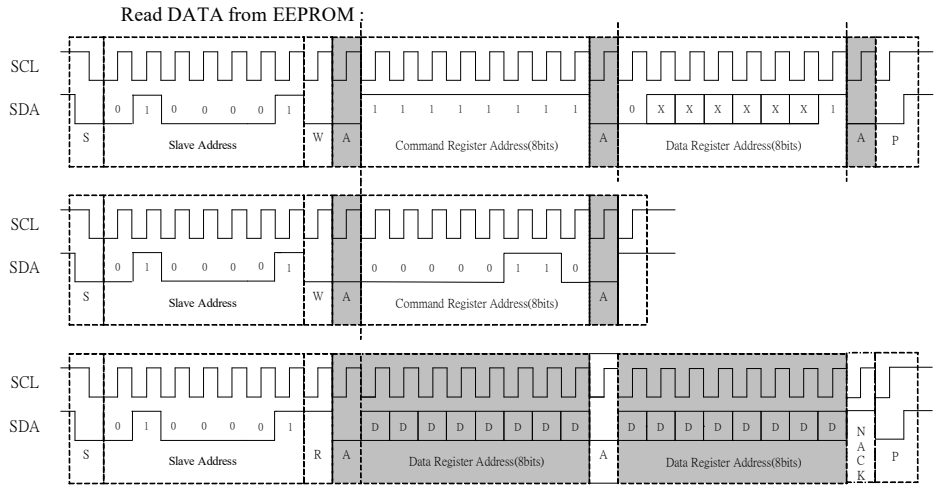
(e) Read Data from EEPROM

Example: Read data from EEPROM address 06h

Step 1: Command for reading EEPROM



☐ From Master to Salve

☐ From Slave to Master

☒ Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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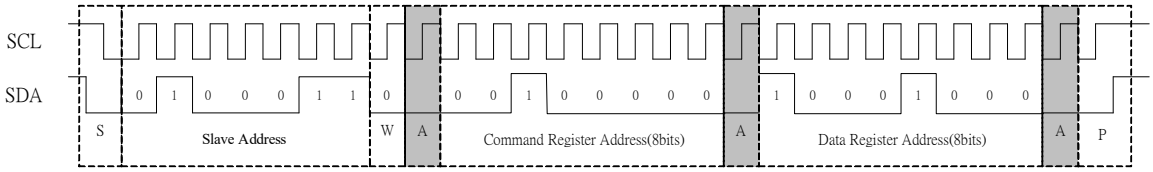
I2C Protocol for PMIC (版本2. 有Write protect)

For A0 bit = 0

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
Slave address (23h, 7-bit) Read=1/Write=0	0	1	0	0	0	1	1	R/W	46h (8-bit)

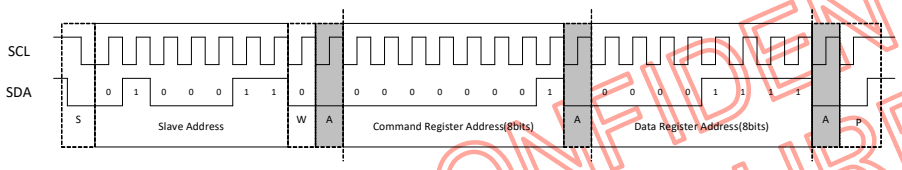
(a) Unlock Write Protect

unlock



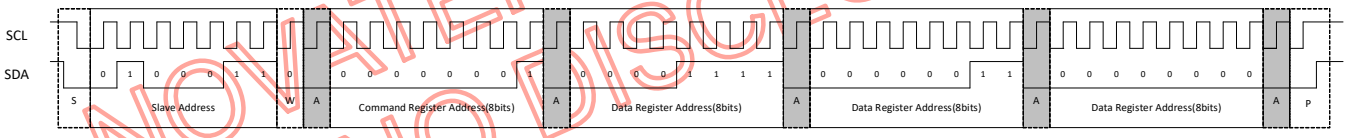
(b) Write Single Byte to DAC

Example: Write Data: 0Fh into DAC address 01h



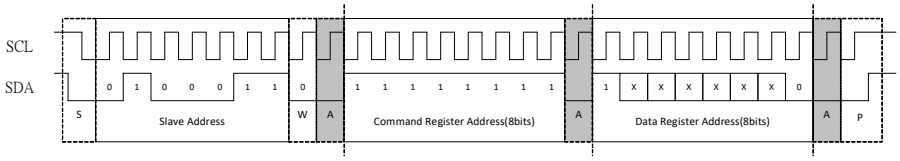
(c) Write Multiple Bytes to DAC

Example: Write Data: 0Fh, 03h, 00h into DAC address 01h, 02h, 03h...



(d) Write all DAC Registers to EEPROM

Example: Write Data: 80h into DAC address FFh



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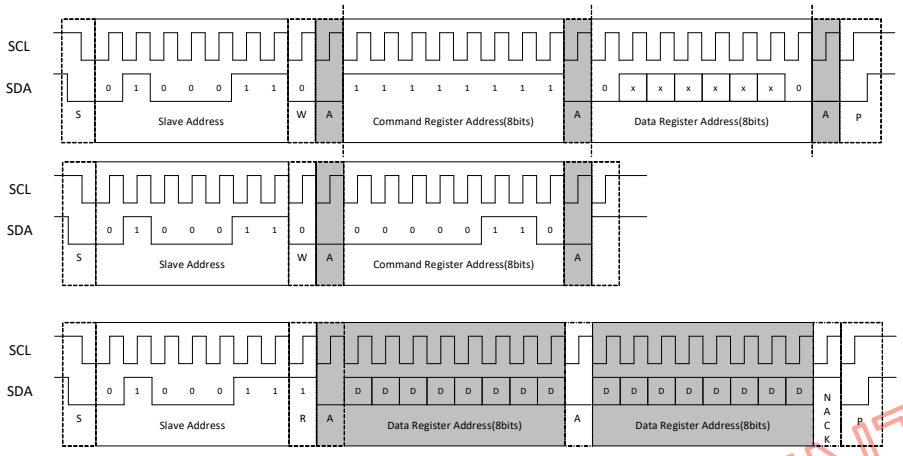
(e) Read Data from DAC

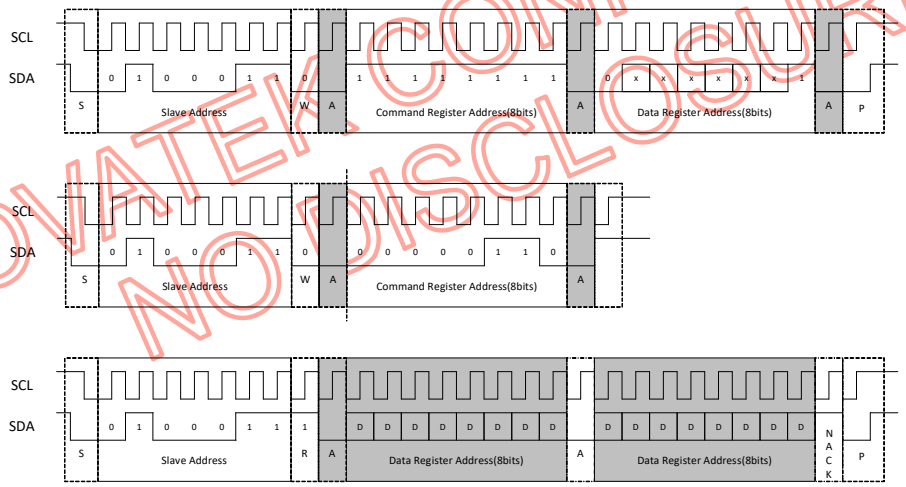
Example: Read data from DAC address 06h



(f) Read Data from EEPROM

Example: Read data from EEPROM address 06h

Step 1: Command for reading EEPROM



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☐ From Master to Salve

■ From Slave to Master

☒ Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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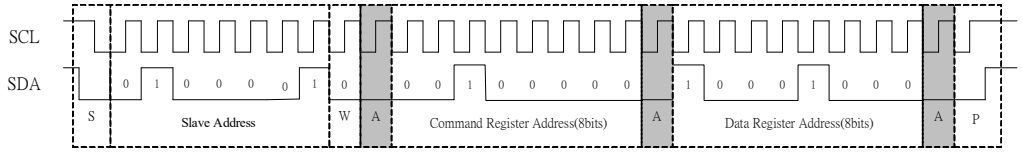
For A0 bit = 1

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
Slave address (21h, 7-bit) Read=1/Write=0	0	1	0	0	0	0	1	R/W	42h (8-bit)

(g) Unlock Write Protect

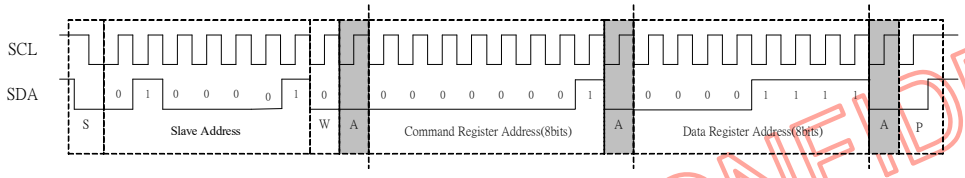
unlock



(h) Write Single Byte to DAC

Example: Write Data: 0Fh into DAC address 01h

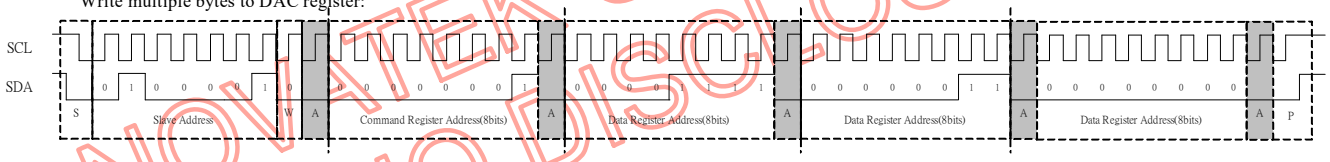
Write single byte to DAC register:



(i) Write Multiple Bytes to DAC

Example: Write Data: 0Fh, 03h, 00h into DAC address 01h, 02h, 03h…

Write multiple bytes to DAC register:



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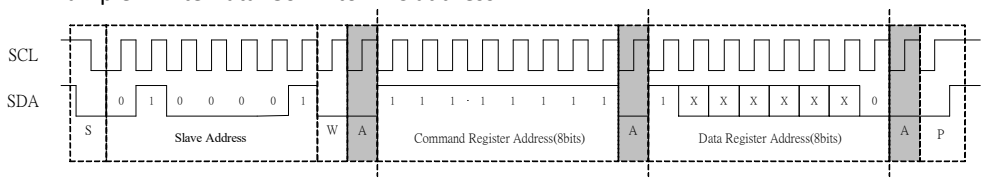
(j) Write all DAC Registers to EEPROM

Example: Write Data: 80h into DAC address FFh



(k) Read Data from DAC

Example: Read data from DAC address 06h

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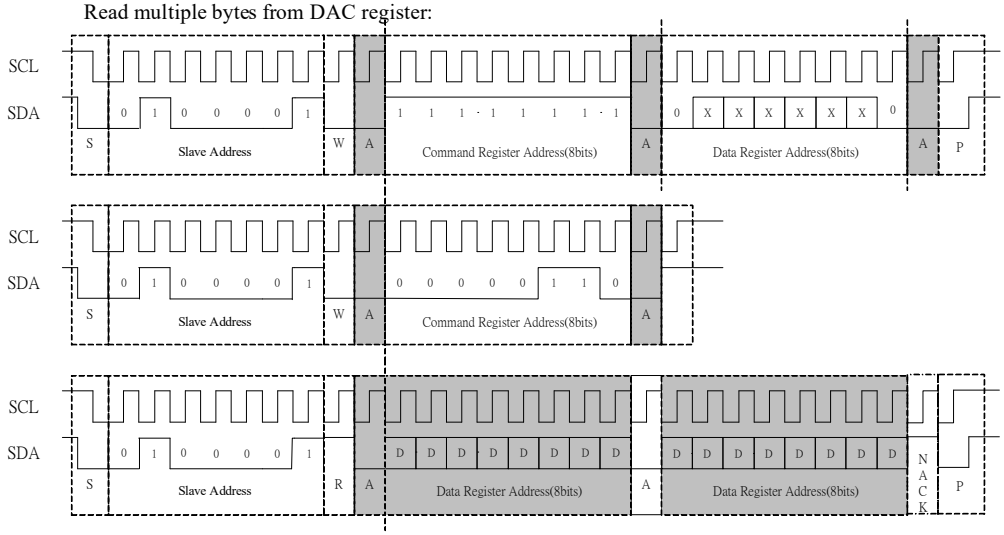
Read multiple bytes from DAC register:

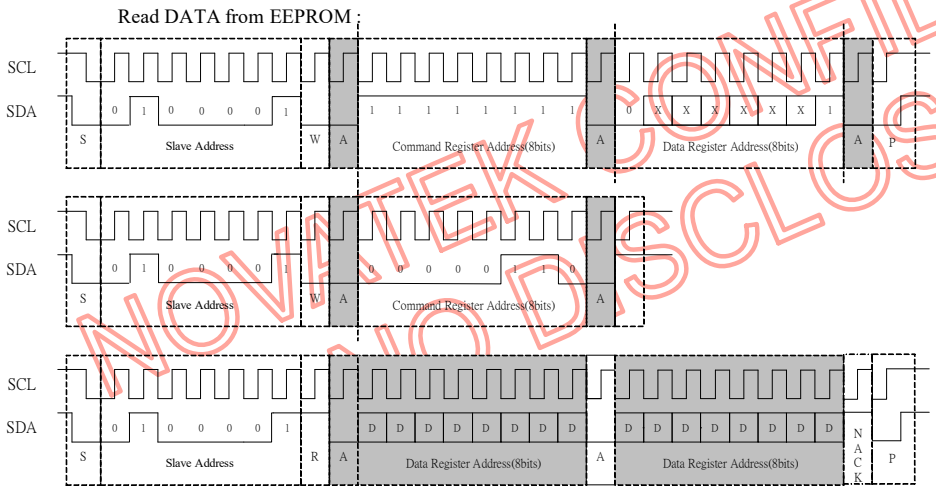


(I) Read Data from EEPROM

Example: Read data from EEPROM address 06h

Step 1: Command for reading EEPROM

Read DATA from EEPROM :



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☐ From Master to Salve

■ From Slave to Master

☒ Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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I2C Protocol for D-VCOM (For A0=0)

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
DVCOM Slave address (4Fh, 7-bit) Read=1/Write=0	1	0	0	1	1	1	1	R/W	9Eh (8-bit)

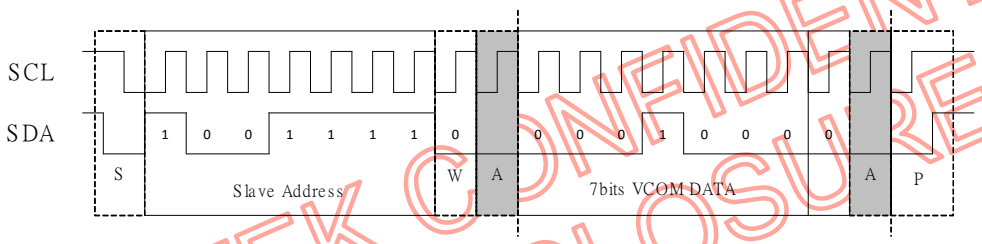
Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
DVCOM Data + 1-bit Data	VCOM[6:0]							CMD	80h

During write command (W=0), (i) set CMD=0 to write data to EEPROM;
(ii) set CMD=1 to write data to DAC.

During read command (R=1), (i) read CMD=1 would show DAC data same to EEPROM;
(ii) read CMD=0 would show DAC data different to EEPROM.

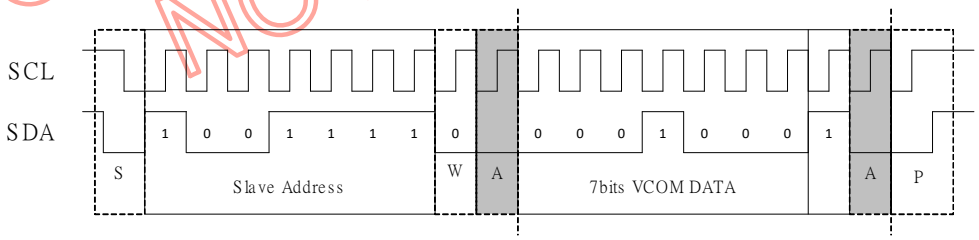
(a) Write Data to EEPROM

Example: Write Data: 08h (7-bit) to EEPROM



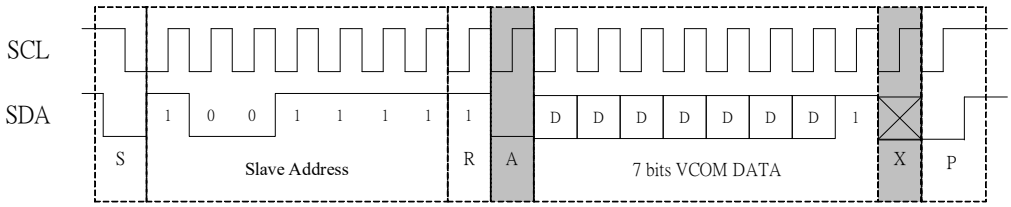
(b) Write Data to DAC

Example: Write Data: 08h (7-bit) to DAC



(c) Read Data from DAC while DAC data is same to EEPROM

Example: Read Data from DAC



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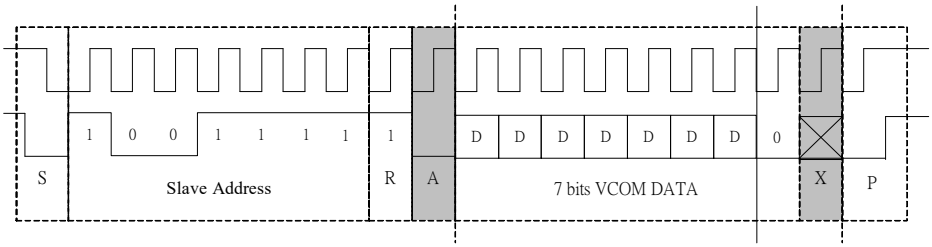
(d) Read Data from DAC while DAC data is different to EEPROM

Example: Read Data from DAC



From Master to Salve

From Slave to Master

Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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I2C Protocol for D-VCOM (For A0=1)

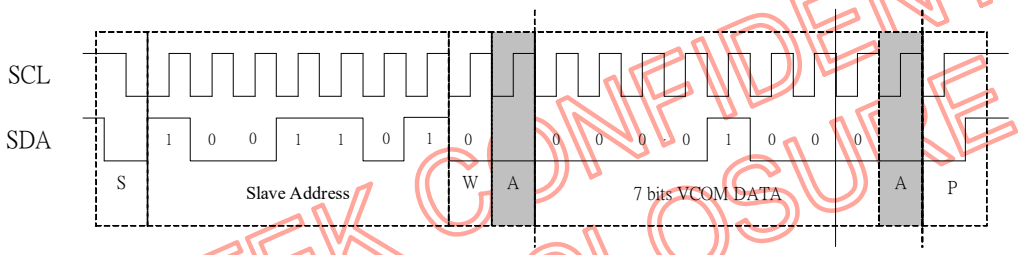
Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
DVCOM Slave address (4Dh, 7-bit) Read=1/Write=0	1	0	0	1	1	0	1	R/W	9Ah (8-bit)

Description	D7	D6	D5	D4	D3	D2	D1	D0	Default
DVCOM Data + 1-bit Data	VCOM[6:0]							CMD	80h

During write command (W=0), (i) set CMD=0 to write data to EEPROM;
(ii) set CMD=1 to write data to DAC.
During read command (R=1), (i) read CMD=1 would show DAC data same to EEPROM;
(ii) read CMD=0 would show DAC data different to EEPROM.

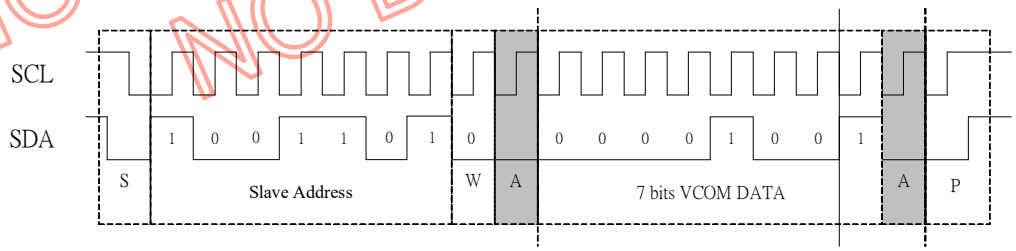
(e) Write Data to EEPROM

Example: Write Data: 04h (7-bit) to EEPROM



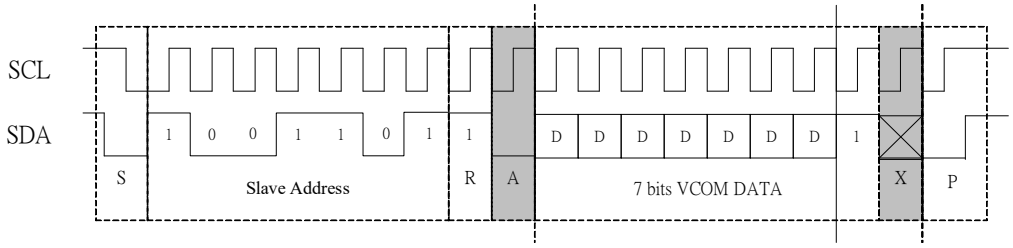
(f) Write Data to DAC

Example: Write Data: 04h (7-bit) to DAC



(g) Read Data from DAC while DAC data is same to EEPROM

Example: Read Data from DAC



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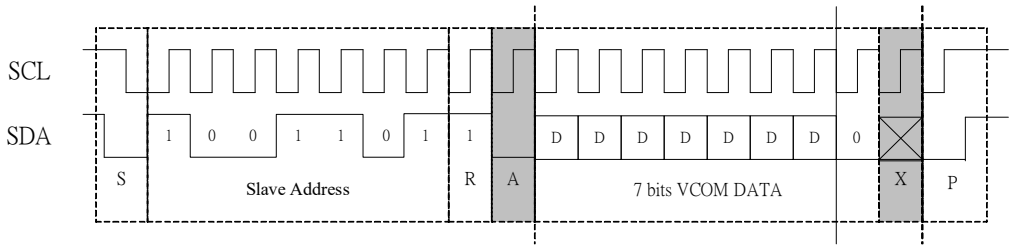
(h) Read Data from DAC while DAC data is different to EEPROM

Example: Read Data from DAC



From Master to Salve

From Slave to Master

Don`t care

A – Acknowledge (SDA Low)

S – START condition

P – STOP condition

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I2C Command List and Description (版本1. No Write protect)

Description	Device Address	D7	D6	D5	D4	D3	D2	D1	D0
PMIC	46h (8-bit)	0	1	0	0	0	1	1	R=1/W=0

紅字為 NT50805 新增 Function，若需與原本 386 共 code ，請將空白處及紅字均填 0

Description	Index Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
Channel Setting	00h	EN_VCOM	EN_LDO	EN_VCORE	EN_VIO	EN_VGL	EN_VGH	EN_AVEE	EN_AVDD	FFh
Channel Setting	01h	VGH_High Resolution	EN_VIO _PWM	EN_VCORE _PWM	PRE_AVDD		EN_RESET	EN_GMA2	EN_GMA1	07h
Channel Setting	02h	VCOM_DISCH	LDO_DISCH	VIO_DISCH	VCORE_DISCH	VGL_DISCH	VGH_DISCH	AVEE_DISCH	AVDD_DISCH	00h
AVDD Voltage	03h	A0		AVDD[5:0]						14h
AVEE Voltage	04h	PIN26_SEL[7:6]			AVEE[4:0]					05h
VGH Voltage	05h	RESET1_CTRL	RESET2_CTRL	VGH_30	VGH[4:0]					0Bh
VGL Voltage	06h	VIN_DISC		VGL[5:0]						08h
VCORE Voltage	07h	AVDD_L_SEL	AVEE_L_SEL	VCORE[5:0]						14h
VIO Voltage	08h	VCORE_L_SEL	VIO_L_SEL	EN_UBRR_LDO	VIO[4:0]					10h
LDO Voltage	09h	EN_UBRR_RESET1	EN_UBRR_RESET2	EN_UBRR_VIO	EN_UBRR_VCORE	LDO[3:0]				08h
VCOM Voltage	0Ah	VCOM[7:1]								80h
VDET Voltage	0Bh	EN_RESET2	VDET2[6:4]				VDET[2:0]			02h
GMA1 Voltage	0Ch			GMA1[5:0]						0Ah
GMA2 Voltage	0Dh			GMA2[5:0]						0Ah
AVDD Boost Configuration	0Eh	LXA_OCP[7:6]		LXA_SR[5:3]			LXA_FREQ[2:0]			61h
AVDD Boost Configuration	0Fh		AVDD_SS[6:4]			AVDD_DLY[3:0]				12h
AVEE Configuration	10h		AVEE_SS[6:4]			AVEE_DLY[2:0]				92h
VGH/VGL SIBO Configuration	11h	SIBO_ENH[7]	LXN SR[6:5]		LXH_SR[4:3]		LXH/N_FREQ[2:0]			12h
VGH/VGL SIBO Configuration	12h	SIBO_FREQH[7]		VGH_SS[5:4]		VGH_DLY[3:0]				05h
VGH/VGL SIBO Configuration	13h		VGL_SS[6:4]			VGL_DLY[3:0]				03h
VCORE Buck Configuration	14h				LXB1_SR[4:3]		LXB1_FREQ[2:0]			15h
VCORE Buck Configuration	15h			VCORE_SS[5:4]		VCORE_DLY[3:0]				11h
VIO Buck Configuration	16h				LXB2_SR[4:3]		LXB2_FREQ[2:0]			15h
VIO Buck Configuration	17h			VIO_SS[5:4]			VIO_DLY[3:0]			12h
RESET Delay	18h	RESET2_DLY[7:4]				RESET_DLY[3:0]				03h
LDO Delay	19h					LDO_DLY[3:0]				02h
VCOM Configuration	1Ah		VCOM_FAST_DISC	VCOM_OFF_SEL	VCOM_DLY[4:0]					05h
AVEE Configuration	1Bh		LXI_SR[6:5]		LXI_OCP[4:3]		Version Code[2:0]			48h
VCOM_MIN	1Ch	VCORE_FREQ_H			VCOM_MIN[4:0]					16h
BOOST PWM control	1Dh		AVEE_PWM	AVDD_PWM						00h
UBRR WP	21h	UBRR WP[7:0]								
UBRR	22h	UBRR								
Write Command (0x0A)	FEh					WED_VCOM				-
Read Write Command	FFh	WED_ALL							RED	00h

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I2C Command List and Description (版本2. 有Write protect)

Description	Device Address	D7	D6	D5	D4	D3	D2	D1	D0
PMIC	46h (8-bit)	0	1	0	0	0	1	1	R=1/W=0

紅字為 NT50805 新增 Function，若需與原本 386 共 code ，請將空白處及紅字均填 0

Description	Index Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
Channel Setting	00h	EN_VCOM	EN_LDO	EN_VCORE	EN_VIO	EN_VGL	EN_VGH	EN_AVEE	EN_AVDD	FFh
Channel Setting	01h	VGH_High Resolution	EN_VIO _PWM	EN_VCORE _PWM	PRE_AVDD		EN_RESET	EN_GMA2	EN_GMA1	07h
Channel Setting	02h	VCOM_DISCH	LDO_DISCH	VIO_DISCH	VCORE_DISCH	VGL_DISCH	VGH_DISCH	AVEE_DISCH	AVDD_DISCH	00h
AVDD Voltage	03h	A0		AVDD[5:0]						14h
AVEE Voltage	04h	PIN26_SEL[7:6]			AVEE[4:0]					05h
VGH Voltage	05h	RESET1_CTRL	RESET2_CTRL	VGH_30	VGH[4:0]					0Bh
VGL Voltage	06h	VIN_DISC		VGL[5:0]						08h
VCORE Voltage	07h	AVDD_L_SEL	AVEE_L_SEL	VCORE[5:0]						14h
VIO Voltage	08h	VCORE_L_SEL	VIO_L_SEL	EN_UBRR_LDO	VIO[4:0]					10h
LDO Voltage	09h	EN_UBRR_RESET1	EN_UBRR_RESET2	EN_UBRR_VIO	EN_UBRR_VCORE	LDO[3:0]				08h
VCOM Voltage	0Ah	VCOM[7:1]								80h
VDET Voltage	0Bh	EN_RESET2	VDET2[6:4]				VDET[2:0]			02h
GMA1 Voltage	0Ch			GMA1[5:0]						0Ah
GMA2 Voltage	0Dh			GMA2[5:0]						0Ah
AVDD Boost Configuration	0Eh	LXA_OCP[7:6]		LXA_SR[5:3]			LXA_FREQ[2:0]			61h
AVDD Boost Configuration	0Fh		AVDD_SS[6:4]			AVDD_DLY[3:0]				12h
AVEE Configuration	10h		AVEE_SS[6:4]			AVEE_DLY[2:0]				92h
VGH/VGL SIBO Configuration	11h	SIBO_ENH[7]	LXN SR[6:5]		LXH_SR[4:3]		LXH/N_FREQ[2:0]			12h
VGH/VGL SIBO Configuration	12h	SIBO_FREQH[7]		VGH_SS[5:4]		VGH_DLY[3:0]				05h
VGH/VGL SIBO Configuration	13h		VGL_SS[6:4]			VGL_DLY[3:0]				03h
VCORE Buck Configuration	14h				LXB1_SR[4:3]		LXB1_FREQ[2:0]			15h
VCORE Buck Configuration	15h			VCORE_SS[5:4]		VCORE_DLY[3:0]				11h
VIO Buck Configuration	16h				LXB2_SR[4:3]		LXB2_FREQ[2:0]			15h
VIO Buck Configuration	17h			VIO_SS[5:4]			VIO_DLY[3:0]			12h
RESET Delay	18h	RESET2_DLY[7:4]				RESET_DLY[3:0]				03h
LDO Delay	19h					LDO_DLY[3:0]				02h
VCOM Configuration	1Ah		VCOM_FAST_DISC	VCOM_OFF_SEL	VCOM_DLY[4:0]					05h
AVEE Configuration	1Bh		LXI_SR[6:5]		LXI_OCP[4:3]		Version Code[2:0]			48h
VCOM_MIN	1Ch	VCORE_FREQ_H			VCOM_MIN[4:0]					16h
BOOST PWM control	1Dh		AVEE_PWM	AVDD_PWM						00h
WP	20h	WP[7:0]								
UBRR WP	21h	UBRR WP[7:0]								
UBRR	22h	UBRR								
Write Command (0x0A)	FEh					WED_VCOM				-
Read Write Command	FFh	WED_ALL							RED	00h

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Table 1-1: Setting Range and Adjustment Step

Symbol	Range	Step	Default Value
AVDD[5:0]	4.0V~7.0V	0.05V	5.0V
AVEE[4:0]	-7.0V~-4.0V	0.1V	-4.5V
VGH[4:0]	6V~12V	0.2V	8.2V
	12.5V~28V	0.5V	18V
VGH_30	CODE=1，Set VGH=28V to 30V	2	28V
VGL[5:0]	-18V~-5.4V	0.2V	-7.0V
VCORE[5:0]	0.8V~2.06V	0.02V	1.2V
VIO[4:0]	1.0V~2.55V	0.05V	1.8V
LDO[3:0]	1.7V~2.8V	0.1V	2.5V
VDET[2:0]	2.0V~2.7V	0.1V	2.2V
GMA1[5:0]	(AVDD)~(AVDD-1.26V)	0.02V	AVDD-0.2V
GMA2[5:0]	(AVEE)~(AVEE+1.26V)	0.02V	AVEE+0.2V
VCOM[7:1]	VCOM_MIN+0V~VCOM_MIN+1.27V	0.01V	VCOM_MIN +0.64V
VCOM_MIN[4:0]	-3.6V~0.75V	0.15V	-0.6V

Table 1-2: Setting Switching Frequency

Symbol	Range
LXA_FREQ[2:0]	600kHz/715kHz/800kHz/933kHz/1000kHz/1225kHz
LXA_SR[5:3]	Level 0~Level 7 (Fast to Slow)
LXA_OCP[7:6]	0.5A/1.0A/1.5A/2.0A
LXH/N_FREQ[2:0]	500kHz/600kHz/715kHz/800kHz/933kHz/1000kHz/1225kHz
LXH_SR[4:3]	Level 0~Level 3 (Fast to Slow)
LXN_SR[6:5]	Level 0~Level 3 (Fast to Slow)
LXB1_FREQ[2:0]	600kHz/715kHz/800kHz/933kHz/1000kHz/1225kHz
LXB1_SR[4:3]	Level 0~Level 3 (Fast to Slow)
LXB2_FREQ[2:0]	600kHz/715kHz/800kHz/933kHz/1000kHz/1225kHz
LXB2_SR[4:3]	Level 0~Level 3 (Fast to Slow)
LXI_OCP[4:3]	1.5A/2.0A/2.5A/3.0A
LXI_SR[6:5]	Level 0~Level 3 (Fast to Slow)

Table 1-3: Power-on and Power-off Delay Setting and Adjustment Step (tolerance would be +/-10%)

Symbol	Range	Step	Default Value
AVDD_DLY[3:0]	0ms~75ms	5ms	10ms
AVDD_SS[6:4]	2ms~16ms	2ms	4ms
AVEE_DLY[3:0]	0ms~75ms	5ms	10ms
AVEE_SS[6:4]	4ms/6ms/8ms/10ms/12ms/14ms/16ms	2ms	4ms
VGH_DLY[3:0]	0ms~75ms	5ms	25ms
VGH_SS[5:4]	4m/6ms/8ms/12ms	2ms	4ms
VGL_DLY[3:0]	0ms~75ms	5ms	15ms
VGL_SS[5:4]	4ms/6ms/8ms/10ms/12ms/14ms/16ms	2ms	4ms
VCORE_DLY[3:0]	0ms~75ms	5ms	5ms
VCORE_SS[6:4]	2ms~8ms	2ms	4ms
VIO_DLY[3:0]	0ms~75ms	5ms	10ms
VIO_SS[6:4]	2ms~8ms	2ms	4ms
RESET_DLY[3:0]	0ms~75ms	5ms	15ms
RESET2_DLY[7:4]	0ms~75ms	5ms	15ms
LDO_DLY[3:0]	0ms~75ms	5ms	10ms
VCOM_DLY[4:0]	0ms~155ms	5ms	25ms

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CMD=00h	Channel Setting								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	1	1	1	1	1	1	1	1	FFh
Parameter	EN_VCOM	EN_LDO	EN_VCORE	EN_VIO	EN_VGL	EN_VGH	EN_AVEE	EN_AVDD	
Default Value:									

Description

--Set the channel setting

Channel Setting		
Symbol	BIN	(V)
EN_VCOM	0	Disable
	1	Enable
EN_LDO	0	Disable
	1	Enable
EN_VCORE	0	Disable
	1	Enable
EN_VIO	0	Disable
	1	Enable
EN_VGL	0	Disable
	1	Enable
EN_VGH	0	Disable
	1	Enable
EN_AVEE	0	Disable
	1	Enable
EN_AVDD	0	Disable
	1	Enable

CMD=01h	Channel Setting.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	1	1	1	07h
Parameter	VGH_High Resolution	EN_VIO _PWM	EN_VCORE _PWM	PRE_AVDD	--	EN_RESET	EN_GMA2	EN_GMA1	
Default Value:									

Description

--Set the channel setting

Channel Setting			
Symbol	BIN	(V)	Description
VGH_High Resolution	0	Disable	VGH=6V-12V
	1	Enable	VGH=12.5V-28V
EN_VIO _PWM	0	Disable	With PSM mode
	1	Enable	VIO is forced to PWM mode
EN_VCORE _PWM	0	Disable	With PSM mode
	1	Enable	VCORE is forced to PWM mode
PRE_AVDD	0	Disable	
	1	Enable	
EN_RESET	0	Disable	
	1	Enable	
EN_GMA2	0	Disable	
	1	Enable	
EN_GMA1	0	Disable	
	1	Enable	

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CMD=02h	Channel Setting.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	0	0	00h
Parameter	VCOM_DISCH	LDO_DISCH	VIO_DISCH	VCORE_DISCH	VGL_DISCH	VGH_DISCH	AVEE_DISCH	AVDD_DISCH	
Default Value:									

Description

--Set the channel setting

Channel Setting			
Symbol	BIN	(V)	Description
VCOM_DISCH	0	Disable	
	1	Enable	VCOM is discharge while power-off
LDO_DISCH	0	Disable	
	1	Enable	LDO is discharge while power-off
VIO_DISCH	0	Disable	
	1	Enable	VIO is discharge while power-off
VCORE_DISCH	0	Disable	
	1	Enable	VCORE is discharge while power-off
VGL_DISCH	0	Disable	
	1	Enable	VGL is discharge while power-off
VGH_DISCH	0	Disable	
	1	Enable	VGH is discharge while power-off
AVEE_DISCH	0	Disable	
	1	Enable	AVEE is discharge while power-off
AVDD_DISCH	0	Disable	
	1	Enable	AVDD is discharge while power-off

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CMD=03h	AVDD Voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	1	0	0	14h
Parameter	A0		AVDD[5]	AVDD[4]	AVDD[3]	AVDD[2]	AVDD[1]	AVDD[0]	
Default Value:									

Description

--Set device address

Device address setting		
Synbol	BIN	Description
A0	0	Device address=0x46(W)，D-VCOM address=0x9E(W)
	1	Device address=0x42(W)，D-VCOM address=0x9A (W)

--Set the AVDD voltage

AVDD[5:0]			AVDD[5:0]		
DEC	BIN	(V)	DEC	BIN	(V)
0	000000	4.00	32	100000	5.60
1	000001	4.05	33	100001	5.65
2	000010	4.10	34	100010	5.70
3	000011	4.15	35	100011	5.75
4	000100	4.20	36	100100	5.80
5	000101	4.25	37	100101	5.85
6	000110	4.30	38	100110	5.90
7	000111	4.35	39	100111	5.95
8	001000	4.40	40	101000	6.00
9	001001	4.45	41	101001	6.05
10	001010	4.50	42	101010	6.10
11	001011	4.55	43	101011	6.15
12	001100	4.60	44	101100	6.20
13	001101	4.65	45	101101	6.25
14	001110	4.70	46	101110	6.30
15	001111	4.75	47	101111	6.35
16	010000	4.80	48	110000	6.40
17	010001	4.85	49	110001	6.45
18	010010	4.90	50	110010	6.50
19	010011	4.95	51	110011	6.55
20	010100	5.00	52	110100	6.60
21	010101	5.05	53	110101	6.65
22	010110	5.10	54	110110	6.70
23	010111	5.15	55	110111	6.75
24	011000	5.20	56	111000	6.80
25	011001	5.25	57	111001	6.85
26	011010	5.30	58	111010	6.90
27	011011	5.35	59	111011	6.95
28	011100	5.40	60	111100	7.00
29	011101	5.45	61	111101	7.00
30	011110	5.50	62	111110	7.00
31	011111	5.55	63	111111	7.00

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CMD=04h	AVEE Voltage								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	1	0	1	05h
Parameter	PIN26_selection[7:6]		-	AVEE[4]	AVEE[3]	AVEE[2]	AVEE[1]	AVEE[0]	
Default Value: AVEE=-4.5V									

Description

--Set PIN26 Function

PIN 26 Function [7:6]		
DEC	BIN	Function
0	00	HI_Z
1	01	RESET2
2	10	UBRR_Hardware control
3	11	UBRR_Hardware control

--Set the AVEE Voltage

AVEE[4:0]		
DEC	BIN	(V)
0	00000	-4.00
1	00001	-4.10
2	00010	-4.20
3	00011	-4.30
4	00100	-4.40
5	00101	-4.50
6	00110	-4.60
7	00111	-4.70
8	01000	-4.80
9	01001	-4.90
10	01010	-5.00
11	01011	-5.10
12	01100	-5.20
13	01101	-5.30
14	01110	-5.40
15	01111	-5.50
16	10000	-5.60
17	10001	-5.70
18	10010	-5.80
19	10011	-5.90
20	10100	-6.00
21	10101	-6.10
22	10110	-6.20
23	10111	-6.30
24	11000	-6.40
25	11001	-6.50
26	11010	-6.60
27	11011	-6.70
28	11100	-6.80
29	11101	-6.90
30	11110	-7.00
31	11111	-7.00

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CMD=05h	VGH Voltage								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	1	0	1	1	0Bh
Parameter	RESET1_CTRL	RESET2_CTRL-	VGH_30	VGH[4]	VGH[3]	VGH[2]	VGH[1]	VGH[0]	
Default Value: VGH=8.2V									

Description

--Set the status when RESET1 disable

BIN	function
0	When Reset1 sets disable, RESET1 is floating
1	When Reset1 sets disable, RESET1 is pull to GND

--Set the status when RESET1 disable

BIN	function
0	When Reset2 sets disable, RESET2 is floating
1	When Reset2 sets disable, RESET2 is pull to GND

--Set the VGH voltage is 30V

BIN	function
0	VGH voltage follows the setting of VGH [4:0]
1	VGH Voltage =30V, while 0x05 D[4] to D[0]=11111 (28V) VGH Voltage follows the setting of 0x05 D[4:0] , while 0x05 D[4] to D[0] is not 11111 (28V),

--Set the VGH Voltage

VGH[4:0] VGH_High_Resolution=0		
DEC	BIN	(V)
0	00000	6.0
1	00001	6.2
2	00010	6.4
3	00011	6.6
4	00100	6.8
5	00101	7.0
6	00110	7.2
7	00111	7.4
8	01000	7.6
9	01001	7.8
10	01010	8.0
11	01011	8.2
12	01100	8.4
13	01101	8.6
14	01110	8.8
15	01111	9.0
16	10000	9.2
17	10001	9.4
18	10010	9.6
19	10011	9.8
20	10100	10.0
21	10101	10.2
22	10110	10.4
23	10111	10.6
24	11000	10.8
25	11001	11.0
26	11010	11.2
27	11011	11.4
28	11100	11.6
29	11101	11.8
30	11110	12.0
31	11111	12.0

VGH[4:0] VGH_High_Resolution=1		
DEC	BIN	(V)
0	00000	12.5
1	00001	13.0
2	00010	13.5
3	00011	14.0
4	00100	14.5
5	00101	15.0
6	00110	15.5
7	00111	16.0
8	01000	16.5
9	01001	17.0
10	01010	17.5
11	01011	18.0
12	01100	18.5
13	01101	19.0
14	01110	19.5
15	01111	20.0
16	10000	20.5
17	10001	21.0
18	10010	21.5
19	10011	22.0
20	10100	22.5
21	10101	23.0
22	10110	23.5
23	10111	24.0
24	11000	24.5
25	11001	25.0
26	11010	25.5
27	11011	26.0
28	11100	26.5
29	11101	27.0
30	11110	27.5
31	11111	28.0

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CMD=06h	VGL Voltage								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	1	0	0	0	08h
Parameter	VIN_DISC	-	VGL[5]	VGL[4]	VGL[3]	VGL[2]	VGL[1]	VGL[0]	
Default Value: VGL=-7V									

Description

--Set the VIN discharge function

BIN	VIN Discharge
0	Disable
1	Enable

--Set the VGL Voltage

VGL[5:0]			VGL[5:0]		
DEC	BIN	(V)	DEC	BIN	(V)
0	000000	-5.40	32	100000	-11.80
1	000001	-5.60	33	100001	-12.00
2	000010	-5.80	34	100010	-12.20
3	000011	-6.00	35	100011	-12.40
4	000100	-6.20	36	100100	-12.60
5	000101	-6.40	37	100101	-12.80
6	000110	-6.60	38	100110	-13.00
7	000111	-6.80	39	100111	-13.20
8	001000	-7.00	40	101000	-13.40
9	001001	-7.20	41	101001	-13.60
10	001010	-7.40	42	101010	-13.80
11	001011	-7.60	43	101011	-14.00
12	001100	-7.80	44	101100	-14.20
13	001101	-8.00	45	101101	-14.40
14	001110	-8.20	46	101110	-14.60
15	001111	-8.40	47	101111	-14.80
16	010000	-8.60	48	110000	-15.00
17	010001	-8.80	49	110001	-15.20
18	010010	-9.00	**50**	**110010**	-15.40
19	010011	-9.20	51	110011	-15.60
20	010100	-9.40	52	110100	-15.80
21	010101	-9.60	53	110101	-16.00
22	010110	-9.80	54	110110	-16.20
23	010111	-10.00	55	110111	-16.40
24	011000	-10.20	56	111000	-16.60
25	011001	-10.40	57	111001	-16.80
26	011010	-10.60	58	111010	-17.00
27	011011	-10.80	59	111011	-17.20
28	011100	-11.00	60	111100	-17.40
29	011101	-11.20	61	111101	-17.60
30	011110	-11.40	62	111110	-17.80
31	011111	-11.60	63	111111	-18.00

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CMD=07h	VCORE voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	1	0	0	14h
Parameter	AVDD_L_SEL	AVEE_L_SEL	VCORE[5]	VCORE[4]	VCORE[3]	VCORE[2]	VCORE[1]	VCORE[0]	
Default Value: VCORE=1.2V									

Description

--Set the Inductor of AVDD block

BIN	Inductor
0	10uH
1	4.7uH

--Set the Inductor of AVEE block

BIN	Inductor
0	10uH
1	4.7uH

--Set the VCORE voltage

VCORE[5:0]			VCORE[5:0]		
DEC	BIN	(V)	DEC	BIN	(V)
0	000000	0.80	32	100000	1.44
1	000001	0.82	33	100001	1.46
2	000010	0.84	34	100010	1.48
3	000011	0.86	35	100011	1.50
4	000100	0.88	36	100100	1.52
5	000101	0.90	37	100101	1.54
6	000110	0.92	38	100110	1.56
7	000111	0.94	39	100111	1.58
8	001000	0.96	40	101000	1.60
9	001001	0.98	41	101001	1.62
10	001010	1.00	42	101010	1.64
11	001011	1.02	43	101011	1.66
12	001100	1.04	44	101100	1.68
13	001101	1.06	45	101101	1.70
14	001110	1.08	46	101110	1.72
15	001111	1.10	47	101111	1.74
16	010000	1.12	48	110000	1.76
17	010001	1.14	49	110001	1.78
18	010010	1.16	50	110010	1.80
19	010011	1.18	51	110011	1.82
20	010100	1.20	52	110100	1.84
21	010101	1.22	53	110101	1.86
22	010110	1.24	54	110110	1.88
23	010111	1.26	55	110111	1.90
24	011000	1.28	56	111000	1.92
25	011001	1.30	57	111001	1.94
26	011010	1.32	58	111010	1.96
27	011011	1.34	59	111011	1.98
28	011100	1.36	60	111100	2.00
29	011101	1.38	61	111101	2.02
30	011110	1.40	62	111110	2.04
31	011111	1.42	63	111111	2.06

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CMD=08h	VIO voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	0	0	0	10h
Parameter	VCORE_L_SEL	VIO_L_SEL	EN_UBRR_LDO	VIO[4]	VIO[3]	VIO[2]	VIO[1]	VIO[0]	
Default Value: VIO=1.8V									

Description

--Set the Inductor of VCORE block

BIN	Inductor
0	4.7uH
1	2.2uH

--Set the Inductor of VIO block

BIN	Inductor
0	4.7uH
1	2.2uH

--Function control of LDO UBRR

BIN	UBRR of LDO
0	Disable
1	Enable

-Set the VIO voltage

VIO[4:0]		
DEC	BIN	(V)
0	00000	1.00
1	00001	1.05
2	00010	1.10
3	00011	1.15
4	00100	1.20
5	00101	1.25
6	00110	1.30
7	00111	1.35
8	01000	1.40
9	01001	1.45
10	01010	1.50
11	01011	1.55
12	01100	1.60
13	01101	1.65
14	01110	1.70
15	01111	1.75
16	10000	1.80
17	10001	1.85
18	10010	1.90
19	10011	1.95
20	10100	2.00
21	10101	2.05
22	10110	2.10
23	10111	2.15
24	11000	2.20
25	11001	2.25
26	11010	2.30
27	11011	2.35
28	11100	2.40
29	11101	2.45
30	11110	2.50
31	11111	2.55

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CMD=09h	LDO voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	1	0	0	0	08h
Parameter	EN_UBRR_RESET1	EN_UBRR_RESET2-	EN_UBRR_VIO-	EN_UBRR_VCORE-	LDO[3]	LDO[2]	LDO[1]	LDO[0]	
Default Value: LDO=2.5V									

Description

--Function control of RESET1 UBRR

BIN	UBRR of RESET1
0	Disable
1	Enable

--Function control of RESET2 UBRR

BIN	UBRR of RESET2
0	Disable
1	Enable

--Function control of VIO UBRR

BIN	UBRR of VIO
0	Disable
1	Enable

--Function control of VCORE UBRR

BIN	UBRR of VCORE
0	Disable
1	Enable

--Set the LDO voltage

LDO[3:0]		
DEC	BIN	(V)
0	0000	1.70
1	0001	1.80
2	0010	1.90
3	0011	2.00
4	0100	2.10
5	0101	2.20
6	0110	2.30
7	0111	2.40
8	1000	2.50
9	1001	2.60
10	1010	2.70
11	1011	2.80
12	1100	2.80
13	1101	2.80
14	1110	2.80
15	1111	2.80

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CMD=0Ah	VCOM Voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	1	0	0	0	0	0	0	-	80h
Parameter	VCOM[7]	VCOM[6]	VCOM[5]	VCOM[4]	VCOM[3]	VCOM[2]	VCOM[1]	-	
Default Value: VCOM_MIN+0.64									

Description

--Set VCOM voltage

VCOM[7:1]			VCOM[7:1]			VCOM[7:1]			VCOM[7:1]		
DEC	BIN	(V)	DEC	BIN	(V)	DEC	BIN	(V)	DEC	BIN	(V)
0	0000000	VCOM_MIN+0.00	32	0100000	VCOM_MIN+0.32	64	1000000	VCOM_MIN+0.64	96	1100000	VCOM_MIN+0.96
1	0000001	VCOM_MIN+0.01	33	0100001	VCOM_MIN+0.33	65	1000001	VCOM_MIN+0.65	97	1100001	VCOM_MIN+0.97
2	0000010	VCOM_MIN+0.02	34	0100010	VCOM_MIN+0.34	66	1000010	VCOM_MIN+0.66	98	1100010	VCOM_MIN+0.98
3	0000011	VCOM_MIN+0.03	35	0100011	VCOM_MIN+0.35	67	1000011	VCOM_MIN+0.67	99	1100011	VCOM_MIN+0.99
4	0000100	VCOM_MIN+0.04	36	0100100	VCOM_MIN+0.36	68	1000100	VCOM_MIN+0.68	100	1100100	VCOM_MIN+1.00
5	0000101	VCOM_MIN+0.05	37	0100101	VCOM_MIN+0.37	69	1000101	VCOM_MIN+0.69	101	1100101	VCOM_MIN+1.01
6	0000110	VCOM_MIN+0.06	38	0100110	VCOM_MIN+0.38	70	1000110	VCOM_MIN+0.70	102	1100110	VCOM_MIN+1.02
7	0000111	VCOM_MIN+0.07	39	0100111	VCOM_MIN+0.39	71	1000111	VCOM_MIN+0.71	103	1100111	VCOM_MIN+1.03
8	0001000	VCOM_MIN+0.08	40	0101000	VCOM_MIN+0.40	72	1001000	VCOM_MIN+0.72	104	1101000	VCOM_MIN+1.04
9	0001001	VCOM_MIN+0.09	41	0101001	VCOM_MIN+0.41	73	1001001	VCOM_MIN+0.73	105	1101001	VCOM_MIN+1.05
10	0001010	VCOM_MIN+0.10	42	0101010	VCOM_MIN+0.42	74	1001010	VCOM_MIN+0.74	106	1101010	VCOM_MIN+1.06
11	0001011	VCOM_MIN+0.11	43	0101011	VCOM_MIN+0.43	75	1001011	VCOM_MIN+0.75	107	1101011	VCOM_MIN+1.07
12	0001100	VCOM_MIN+0.12	44	0101100	VCOM_MIN+0.44	76	1001100	VCOM_MIN+0.76	108	1101100	VCOM_MIN+1.08
13	0001101	VCOM_MIN+0.13	45	0101101	VCOM_MIN+0.45	77	1001101	VCOM_MIN+0.77	109	1101101	VCOM_MIN+1.09
14	0001110	VCOM_MIN+0.14	46	0101110	VCOM_MIN+0.46	78	1001110	VCOM_MIN+0.78	110	1101110	VCOM_MIN+1.10
15	0001111	VCOM_MIN+0.15	47	0101111	VCOM_MIN+0.47	79	1001111	VCOM_MIN+0.79	111	1101111	VCOM_MIN+1.11
16	0010000	VCOM_MIN+0.16	48	0110000	VCOM_MIN+0.48	80	1010000	VCOM_MIN+0.80	112	1110000	VCOM_MIN+1.12
17	0010001	VCOM_MIN+0.17	49	0110001	VCOM_MIN+0.49	81	1010001	VCOM_MIN+0.81	113	1110001	VCOM_MIN+1.13
18	0010010	VCOM_MIN+0.18	50	0110010	VCOM_MIN+0.50	82	1010010	VCOM_MIN+0.82	114	1110010	VCOM_MIN+1.14
19	0010011	VCOM_MIN+0.19	51	0110011	VCOM_MIN+0.51	83	1010011	VCOM_MIN+0.83	115	1110011	VCOM_MIN+1.15
20	0010100	VCOM_MIN+0.20	52	0110100	VCOM_MIN+0.52	84	1010100	VCOM_MIN+0.84	116	1110100	VCOM_MIN+1.16
21	0010101	VCOM_MIN+0.21	53	0110101	VCOM_MIN+0.53	85	1010101	VCOM_MIN+0.85	117	1110101	VCOM_MIN+1.17
22	0010110	VCOM_MIN+0.22	54	0110110	VCOM_MIN+0.54	86	1010110	VCOM_MIN+0.86	118	1110110	VCOM_MIN+1.18
23	0010111	VCOM_MIN+0.23	55	0110111	VCOM_MIN+0.55	87	1010111	VCOM_MIN+0.87	119	1110111	VCOM_MIN+1.19
24	0011000	VCOM_MIN+0.24	56	0111000	VCOM_MIN+0.56	88	1011000	VCOM_MIN+0.88	120	1111000	VCOM_MIN+1.20
25	0011001	VCOM_MIN+0.25	57	0111001	VCOM_MIN+0.57	89	1011001	VCOM_MIN+0.89	121	1111001	VCOM_MIN+1.21
26	0011010	VCOM_MIN+0.26	58	0111010	VCOM_MIN+0.58	90	1011010	VCOM_MIN+0.90	122	1111010	VCOM_MIN+1.22
27	0011011	VCOM_MIN+0.27	59	0111011	VCOM_MIN+0.59	91	1011011	VCOM_MIN+0.91	123	1111011	VCOM_MIN+1.23
28	0011100	VCOM_MIN+0.28	60	0111100	VCOM_MIN+0.60	92	1011100	VCOM_MIN+0.92	124	1111100	VCOM_MIN+1.24
29	0011101	VCOM_MIN+0.29	61	0111101	VCOM_MIN+0.61	93	1011101	VCOM_MIN+0.93	125	1111101	VCOM_MIN+1.25
30	0011110	VCOM_MIN+0.30	62	0111110	VCOM_MIN+0.62	94	1011110	VCOM_MIN+0.94	126	1111110	VCOM_MIN+1.26
31	0011111	VCOM_MIN+0.31	63	0111111	VCOM_MIN+0.63	95	1011111	VCOM_MIN+0.95	127	1111111	VCOM_MIN+1.27

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CMD=0Bh	VDET voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	1	0	02h
Parameter	EN_RESET2	VDET2[6]	VDET2[5]	VDET2[4]	-	VDET[2]	VDET[1]	VDET[0]	
Default Value: VDET=2.2V									

Description

--Set the channel setting

Channel Setting		
Symbol	BIN	(V)
EN_RESET2	0	Disable
	1	Enable

--Set the VDET2 voltage

VDET2[2:0]		
DEC	BIN	(V)
0	000	2.00
1	001	2.10
2	010	2.20
3	011	2.30
4	100	2.40
5	101	2.50
6	110	2.60
7	111	2.70

--Set the VDET voltage

VDET[2:0]		
DEC	BIN	(V)
0	000	2.00
1	001	2.10
2	010	2.20
3	011	2.30
4	100	2.40
5	101	2.50
6	110	2.60
7	111	2.70

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CMD=0Ch	GMA1 voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	1	0	1	0	0Ah
Parameter	-	-	GMA1[5]	GMA1[4]	GMA1[3]	GMA1[2]	GMA1[1]	GMA1[0]	
Default Value:GMA1=AVDD-0.5V									

Description

--Set the GMA1 voltage

GMA1[5:0]			GMA1[5:0]		
DEC	BIN	(V)	DEC	BIN	(V)
0	000000	AVDD	32	100000	AVDD-0.64
1	000001	AVDD-0.02	33	100001	AVDD-0.66
2	000010	AVDD-0.04	34	100010	AVDD-0.68
3	000011	AVDD-0.06	35	100011	AVDD-0.70
4	000100	AVDD-0.08	36	100100	AVDD-0.72
5	000101	AVDD-0.10	37	100101	AVDD-0.74
6	000110	AVDD-0.12	38	100110	AVDD-0.76
7	000111	AVDD-0.14	39	100111	AVDD-0.78
8	001000	AVDD-0.16	40	101000	AVDD-0.80
9	001001	AVDD-0.18	41	101001	AVDD-0.82
10	001010	AVDD-0.20	42	101010	AVDD-0.84
11	001011	AVDD-0.22	43	101011	AVDD-0.86
12	001100	AVDD-0.24	44	101100	AVDD-0.88
13	001101	AVDD-0.26	45	101101	AVDD-0.90
14	001110	AVDD-0.28	46	101110	AVDD-0.92
15	001111	AVDD-0.30	47	101111	AVDD-0.94
16	010000	AVDD-0.32	48	110000	AVDD-0.96
17	010001	AVDD-0.34	49	110001	AVDD-0.98
18	010010	AVDD-0.36	50	110010	AVDD-1.00
19	010011	AVDD-0.38	51	110011	AVDD-1.02
20	010100	AVDD-0.40	52	110100	AVDD-1.04
21	010101	AVDD-0.42	53	110101	AVDD-1.06
22	010110	AVDD-0.44	54	110110	AVDD-1.08
23	010111	AVDD-0.46	55	110111	AVDD-1.10
24	011000	AVDD-0.48	56	111000	AVDD-1.12
25	011001	AVDD-0.50	57	111001	AVDD-1.14
26	011010	AVDD-0.52	58	111010	AVDD-1.16
27	011011	AVDD-0.54	59	111011	AVDD-1.18
28	011100	AVDD-0.56	60	111100	AVDD-1.20
29	011101	AVDD-0.58	61	111101	AVDD-1.22
30	011110	AVDD-0.60	62	111110	AVDD-1.24
31	011111	AVDD-0.62	63	111111	AVDD-1.26

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CMD=0Dh	GMA2 voltage.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	1	0	1	0	0Ah
Parameter	-	-	GMA2[5]	GMA2[4]	GMA2[3]	GMA2[2]	GMA2[1]	GMA2[0]	
Default Value: GMA2=AVEE+0.2V									

Description

--Set the GMA2 voltage

GMA2[5:0]			GMA2[5:0]		
DEC	BIN	(V)	DEC	BIN	(V)
0	000000	AVEE	32	100000	AVEE+0.64
1	000001	AVEE+0.02	33	100001	AVEE+0.66
2	000010	AVEE+0.04	34	100010	AVEE+0.68
3	000011	AVEE+0.06	35	100011	AVEE+0.70
4	000100	AVEE+0.08	36	100100	AVEE+0.72
5	000101	AVEE+0.10	37	100101	AVEE+0.74
6	000110	AVEE+0.12	38	100110	AVEE+0.76
7	000111	AVEE+0.14	39	100111	AVEE+0.78
8	001000	AVEE+0.16	40	101000	AVEE+0.80
9	001001	AVEE+0.18	41	101001	AVEE+0.82
10	001010	AVEE+0.20	42	101010	AVEE+0.84
11	001011	AVEE+0.22	43	101011	AVEE+0.86
12	001100	AVEE+0.24	44	101100	AVEE+0.88
13	001101	AVEE+0.26	45	101101	AVEE+0.90
14	001110	AVEE+0.28	46	101110	AVEE+0.92
15	001111	AVEE+0.30	47	101111	AVEE+0.94
16	010000	AVEE+0.32	48	110000	AVEE+0.96
17	010001	AVEE+0.34	49	110001	AVEE+0.98
18	010010	AVEE+0.36	50	110010	AVEE+1.00
19	010011	AVEE+0.38	51	110011	AVEE+1.02
20	010100	AVEE+0.40	52	110100	AVEE+1.04
21	010101	AVEE+0.42	53	110101	AVEE+1.06
22	010110	AVEE+0.44	54	110110	AVEE+1.08
23	010111	AVEE+0.46	55	110111	AVEE+1.10
24	011000	AVEE+0.48	56	111000	AVEE+1.12
25	011001	AVEE+0.50	57	111001	AVEE+1.14
26	011010	AVEE+0.52	58	111010	AVEE+1.16
27	011011	AVEE+0.54	59	111011	AVEE+1.18
28	011100	AVEE+0.56	60	111100	AVEE+1.20
29	011101	AVEE+0.58	61	111101	AVEE+1.22
30	011110	AVEE+0.60	62	111110	AVEE+1.24
31	011111	AVEE+0.62	63	111111	AVEE+1.26

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CMD=0Eh	AVDD Boost Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	1	1	0	0	0	0	1	61h
Parameter	LXA_OCP[7]	LXA_OCP[6]	LXA_SR[5]	LXA_SR[4]	LXA_SR[3]	LXA_FREQ[2]	LXA_FREQ[1]	LXA_FREQ[0]	
Default Value:									

Description

-- -Set LXA over-current limit

LXA_OCP[7:6]		
DEC	BIN	A
0	00	0.5
1	01	1.0
2	10	1.5
3	11	2.0

-- -Set LXA slew rate

LXA_SR[5:3]		
DEC	BIN	Fast to Slow
0	000	Level 0 (Fastest
1	001	Level 1
2	**010**	Level 2
3	011	Level 3
4	100	Level 4 (Normal)
5	101	Level 5
6	110	Level 6
7	111	Level 7 (Slowest)

--Set AVDD LXA switching frequency.

LXA_FREQ[2:0]		
DEC	BIN	kHz
0	000	600
1	001	715
2	010	800
3	011	933
4	100	1000
5	101	1225
6	110	1225
7	111	1225

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CMD=0Fh	AVDD Boost Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	0	1	0	12h
Parameter		AVDD_SS[6]	AVDD_SS[5]	AVDD_SS[4]	AVDD_DLY[3]	AVDD_DLY[2]	AVDD_DLY[1]	AVDD_DLY[0]	
Default Value:									

Description

-- Set AVDD power-on soft-start time

AVDD_SS[6:4]		
DEC	BIN	ms
0	000	2
1	001	4
2	010	6
3	011	8
4	100	10
5	101	12
6	110	14
7	111	16

--Set AVDD power-on delay time.

AVDD_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=10h	AVEE Charge pump Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	1	0	0	1	0	0	1	0	92h
Parameter	-	AVEE_SS[6]	AVEE_SS[5]	AVEE_SS[4]	AVEE_DLY[3]	AVEE_DLY[2]	AVEE_DLY[1]	AVEE_DLY[0]	
Default Value:									

Description

-- Set AVEE power-on soft-start time

AVEE_SS[6:4]		
DEC	BIN	ms
0	000	4
1	001	4
2	010	6
3	011	8
4	100	10
5	101	12
6	110	14
7	111	16

--Set AVEE power-on delay time.

AVEE_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=11h	VGH/VGL SIBO Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	0	1	0	12h
Parameter	SIBO_ENH[7]	LXN _SR[6]	LXN _SR[5]	LXH _SR[4]	LXH _SR[3]	LXH/N_FREQ[2]	LXH/N_FREQ[1]	LXH/N_FREQ[0]	
Default Value:									

Description

-Set VINP power

SIBO_ENH[7]		
DEC	BIN	
0	0	VINP connect to VIN
1	1	VINP connect to AVDD

-Set LXN slew rate

LXH/N_SR[4:3]		
DEC	BIN	
0	00	Fastest
1	01	Fast
2	10	Normal
3	11	Slow

-- -Set LXH slew rate

LXH/N_SR[4:3]		
DEC	BIN	
0	00	Fastest
1	01	Fast
2	**10**	Normal
3	11	Slow

--Set LXH/N switching frequency.

LXH/N_FREQ[2:0]		
DEC	BIN	kHz
0	000	500
1	001	600
2	**010**	715
3	011	800
4	100	933
5	101	1000
6	110	1225
7	111	1225

-
-

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CMD=12h	VGH/VGL SIBO Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	1	0	1	05h
Parameter	SIBO_FREQH	-	VGH_SS[5]	VGH_SS[4]	VGH_DLY[3]	VGH_DLY[2]	VGH_DLY[1]	VGH_DLY[0]	
Default Value:									

Description

-- Set SIBO to be Low Frequency

SIBO_FREQH **[7]**		
DEC	BIN	Description
0	0	Keep LXN/LXP_FREQ[2:0]
1	1	Set SIBO frequency be 1/2 * LXN/LXP_FREQ[2:0]

-- Set VGH power-on soft-start time

VGH_SS[5:4]		
DEC	BIN	ms
0	00	4
1	01	6
2	10	8
3	11	12

--Set VGH power-on delay time.

VGH_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=13h	VGH/VGL SIBO Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	1	1	03h
Parameter	-	VGL_SS[6]	VGL_SS[5]	VGL_SS[4]	VGL_DLY[3]	VGL_DLY[2]	VGL_DLY[1]	VGL_DLY[0]	
Default Value:									

Description

-- Set VGL power-on soft-start time

VGL_SS[6:4]		
DEC	BIN	ms
0	000	4
1	001	4
2	010	6
3	011	8
4	100	10
5	101	12
6	110	14
7	111	16

--Set VGL power-on delay time.

VGL_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=14h	VCORE Buck Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	1	0	1	15h
Parameter	-	-	-	LXB1_SR [4]	LXB1_SR [3]	LXB1_FREQ [2]	LXB1_FREQ [1]	LXB1_FREQ [0]	
Default Value:									

Description

--Set LXB1 slew rate

LXB1_SR [4:3]		
DEC	BIN	
0	00	Fastest
1	01	Fast
2	10	Normal
3	11	Slow

--Set VCORE LXB1 switching frequency.

LXB1_FREQ [2:0]		
DEC	BIN	kHz
0	000	600
1	001	715
2	010	800
3	011	933
4	100	1000
5	101	1225
6	110	1225
7	111	1225

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CMD=15h	VCORE Buck Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	0	0	1	11h
Parameter	-	-	VCORE _SS [5]	VCORE_SS [4]	VCORE_DLY [3]	VCORE_DLY [2]	VCORE_DLY [1]	VCORE_DLY [0]	
Default Value:									

Description

--Set VCORE power-on soft-start time

VCORE_SS[5:4]		
DEC	BIN	ms
0	00	2
1	01	4
2	10	6
3	11	8

--Set VCORE power-on delay time.

VCORE_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=16h	VIO Buck Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	1	0	1	15h
Parameter	-	-	-	LXB2_SR [4]	LXB2_SR [3]	LXB2_FREQ [2]	LXB2_FREQ [1]	LXB2_FREQ [0]	
Default Value:									

Description

-- Set LXB2 slew rate

LXB2_SR [4:3]		
DEC	BIN	
0	00	Fastest
1	01	Fast
2	10	Normal
3	11	Slow

--Set VIO LXB2 switching frequency.

LXB2_FREQ [2:0]		
DEC	BIN	kHz
0	000	600
1	001	715
2	010	800
3	011	933
4	100	1000
5	101	1225
6	110	1225
7	111	1225

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CMD=17h	VIO Buck Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	0	1	0	12h
Parameter	-	-	VIO_SS [5]	VIO_SS [4]	VIO_DLY [3]	VIO_DLY [2]	VIO_DLY [1]	VIO_DLY [0]	
Default Value:									

Description

-- Set VIO power-on soft-start time

VIO_SS[4:3]		
DEC	BIN	ms
0	00	2
1	01	4
2	10	6
3	11	8

--Set VIO power-on delay time.

VIO_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=18h	XAO Delay								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	1	1	03h
Parameter	RESET2_DLY [7]	RESET2_DLY [6]	RESET2_DLY [5]	RESET2_DLY [4]	RESET_DLY [3]	RESET_DLY [2]	RESET_DLY [1]	RESET_DLY [0]	
Default Value:									

Description

--Set the RESET and RESET2 power-on delay time

RESET2_DLY [3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

RESET_DLY [3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=19h	LDO_DLY								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	1	0	02h
Parameter	-	-	-	-	LDO_DLY [3]	LDO_DLY [2]	LDO_DLY [1]	LDO_DLY [0]	
Default Value:									

Description

--Set LDO power-on delay time.

LDO_DLY[3:0]		
DEC	BIN	ms
0	0000	0
1	0001	5
2	0010	10
3	0011	15
4	0100	20
5	0101	25
6	0110	30
7	0111	35
8	1000	40
9	1001	45
10	1010	50
11	1011	55
12	1100	60
13	1101	65
14	1110	70
15	1111	75

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CMD=1Ah	VCOM Configuration.								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	1	0	1	05h
Parameter		VCOM_FAST_DISC	VCOM_OFF_SEL	VCOM_DLY [4]	VCOM_DLY [3]	VCOM_DLY [2]	VCOM_DLY [1]	VCOM_DLY [0]	
Default Value:									

Description

-- Set VCOM fast discharge

VCOM_FAST_DISC		
DEC	BIN	Function
0	0	Disable
1	1	Enable

-- Set VCOM power-off threshold voltage

VCOM_OFF_SEL		
DEC	BIN	
0	0	UVLO_F
1	1	VDET1

--Set VCOM power-on delay time.

VCOM_DLY [4:0]		
DEC	BIN	ms
0	00000	0
1	00001	5
2	00010	10
3	00011	15
4	00100	20
5	00101	25
6	00110	30
7	00111	35
8	01000	40
9	01001	45
10	01010	50
11	01011	55
12	01100	60
13	01101	65
14	01110	70
15	01111	75
16	10000	80
17	10001	85
18	10010	90
19	10011	95
20	10100	100
21	10101	105
22	10110	110
23	10111	115
24	11000	120
25	11001	125
26	11010	130
27	11011	135
28	11100	140
29	11101	145
30	11110	150
31	11111	155

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CMD=1Bh	AVDD Boost/AVEE CP Configuration								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	1	0	0	1	0	0	0	48h
Parameter		LXI_SR [6]	LXI_SR [5]	LXI_OCP [4]	LXI_OCP [3]	VER_CODE [2]	VER_CODE [1]	VER_CODE [0]	
Default Value:									

Description

-- Set AVEE LXI switching frequency

LXI_SR[6:5]		
DEC	BIN	
0	00	Fastest
1	01	Fast
2	10	**Normal**
3	11	Slow

--Set AVEE LXI Over current limit

LXI_OCP[4:3]		
DEC	BIN	A
0	00	1.5
1	01	2
2	10	2.5
3	11	3

--Set Version Code

VER_CODE[2:0]		
DEC	BIN	
0	000	-
1	001	-
2	010	-
3	011	-
4	100	-
5	**101**	-
6	110	-
7	111	-

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CMD=1Ch	Set minimum VCOM Voltage								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	1	0	1	1	0	16h
Parameter	VCORE_FREQ_H	-		VCOM_MIN [4]	VCOM_MIN [3]	VCOM_MIN [2]	VCOM_MIN [1]	VCOM_MIN [0]	
Default Value:									

Description

--Set the Vcore Frequency

BIN	Vcore frequency
0	Follow 0x14 D[2] to D[0] Setting
1	1.8MHz

--Set the VCOM Voltage

VCOM_MIN[4:0]		
DEC	BIN	(V)
0	00000	-3.600
1	00001	-3.600
2	00010	-3.600
3	00011	-3.450
4	00100	-3.300
5	00101	-3.150
6	00110	-3.000
7	00111	-2.850
8	01000	-2.700
9	01001	-2.550
10	01010	-2.400
11	01011	-2.250
12	01100	-2.100
13	01101	-1.950
14	01110	-1.800
15	01111	-1.650
16	10000	-1.500
17	10001	-1.350
18	10010	-1.200
19	10011	-1.050
20	10100	-0.900
21	10101	-0.750
22	10110	-0.600
23	10111	-0.450
24	11000	-0.300
25	11001	-0.150
26	11010	0.000
27	11011	0.150
28	11100	0.300
29	11101	0.450
30	11110	0.600
31	11111	0.750

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CMD=1Dh	Set minimum VCOM Voltage								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	0	0	00h
Parameter	-	AVEE_PWM	AVDD_PWM	-	-	-	-	-	
Default Value:									

Description	--Set the channel setting

Channel setting			
Symbol	BIN	Condition	Description
EN_AVEE_PWM	0	Disable	With PSM mode
	1	Enable	AVEE is forced to PWM mode
EN_AVDD_PWM	0	Disable	With PSM mode
	1	Enable	AVDD is forced to PWM mode

(0X20 Only for 版本 2 有 Write Protect function)

CMD=20h	Write Protect								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	1	0	0	0	1	0	0	0	88h
Parameter	WP[7]	WP[6]	WP[5]	WP[4]	WP[3]	WP[2]	WP[1]	WP[0]	
Default Value:									

Description	--To disable the Write Protect let WP[7:0]=88h

CMD=21h	UBRR Write Protect								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	1	0	0	0	1	0	0	0	95h
Parameter	UBRR_WP [7]	UBRR_WP [6]	UBRR_WP [5]	UBRR_WP [4]	UBRR_WP [3]	UBRR_WP [2]	UBRR_WP [1]	UBRR_WP [0]	
Default Value:									

Description	--To disable the UBRR Write Protect let UBRR_WP[7:0]=95h

CMD=22h	UBRR software control								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	0	0	0	0	0	0	0	0	00h
Parameter	UBRR								
Default Value:									

Description	-- Software_UBRR Control

BIN	UBRR Function
0	Disable
1	Enable 0X04 D[7:6]=10,11 Then Software_UBRR have no function

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CMD=FEh	WED_VCOM: Write current 0Ah commands to internal EEPROM								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	-	-	-	-	-	-	-	-	-
Parameter	-	-	-	-	WED_VCOM	-	-	-	-

Description

-- Write 0Ah commands to internal EEPROM

WED_VCOM		
DEC	BIN	Condition
0	0	No action
1	1	Write DAC into EEPROM

CMD=FFh	WED: Write current 01h~0Dh commands to internal EEPROM								
Inst / Para	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Default	-	-	-	-	-	-	-	-	
Parameter	WED							RED	

Description

-- Write 00h to 1Ch commands to internal EEPROM

WED		
DEC	BIN	Condition
0	0	No action
1	1	Write DAC into EEPROM

-- Read 00h to 1Ch commands from internal EEPROM

RED		
DEC	BIN	Condition
0	0	Read Data from DAC
1	1	Read EEPROM into DAC

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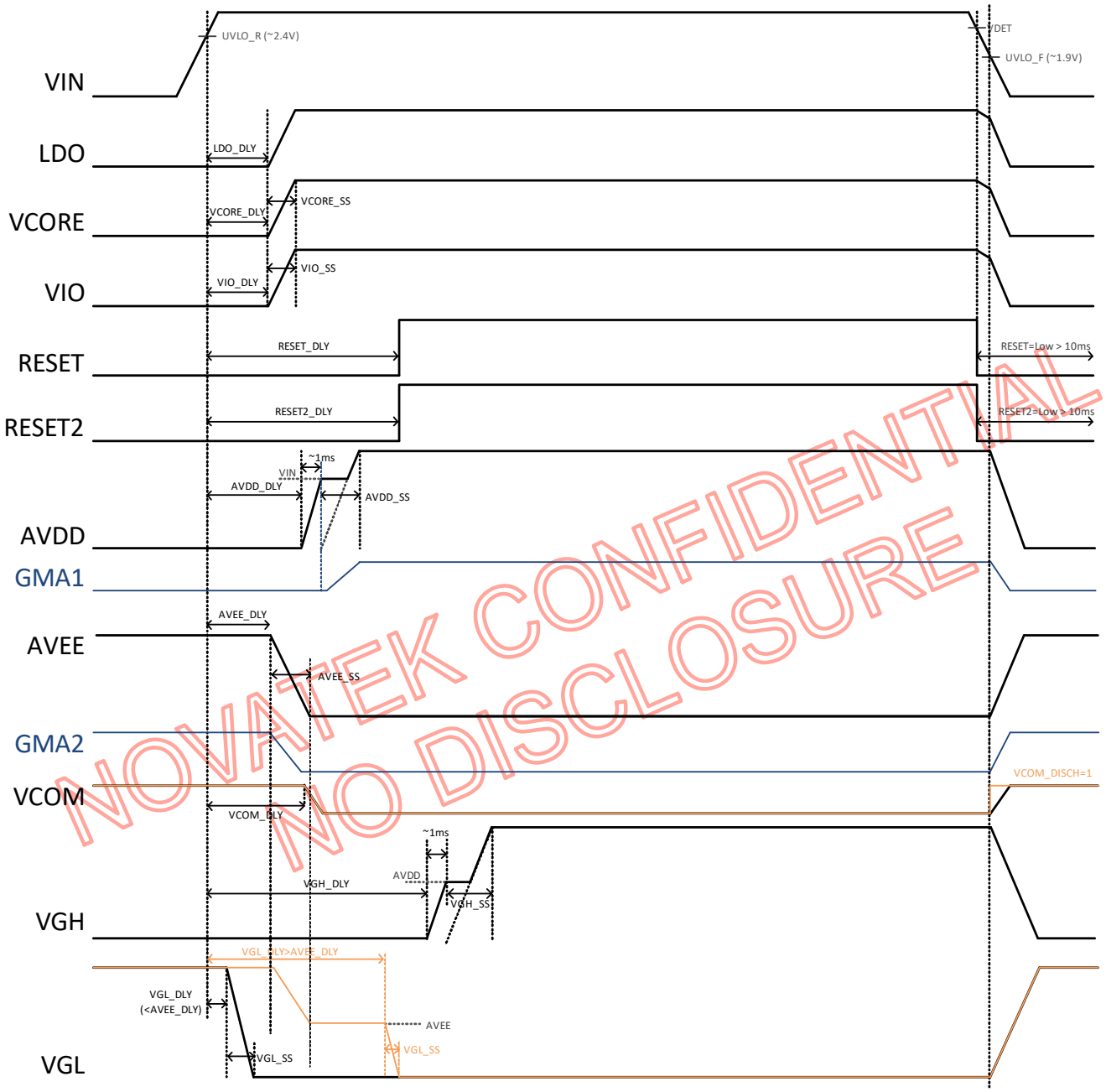
Power ON/OFF Sequence (SIBO VINP from 3.3V)



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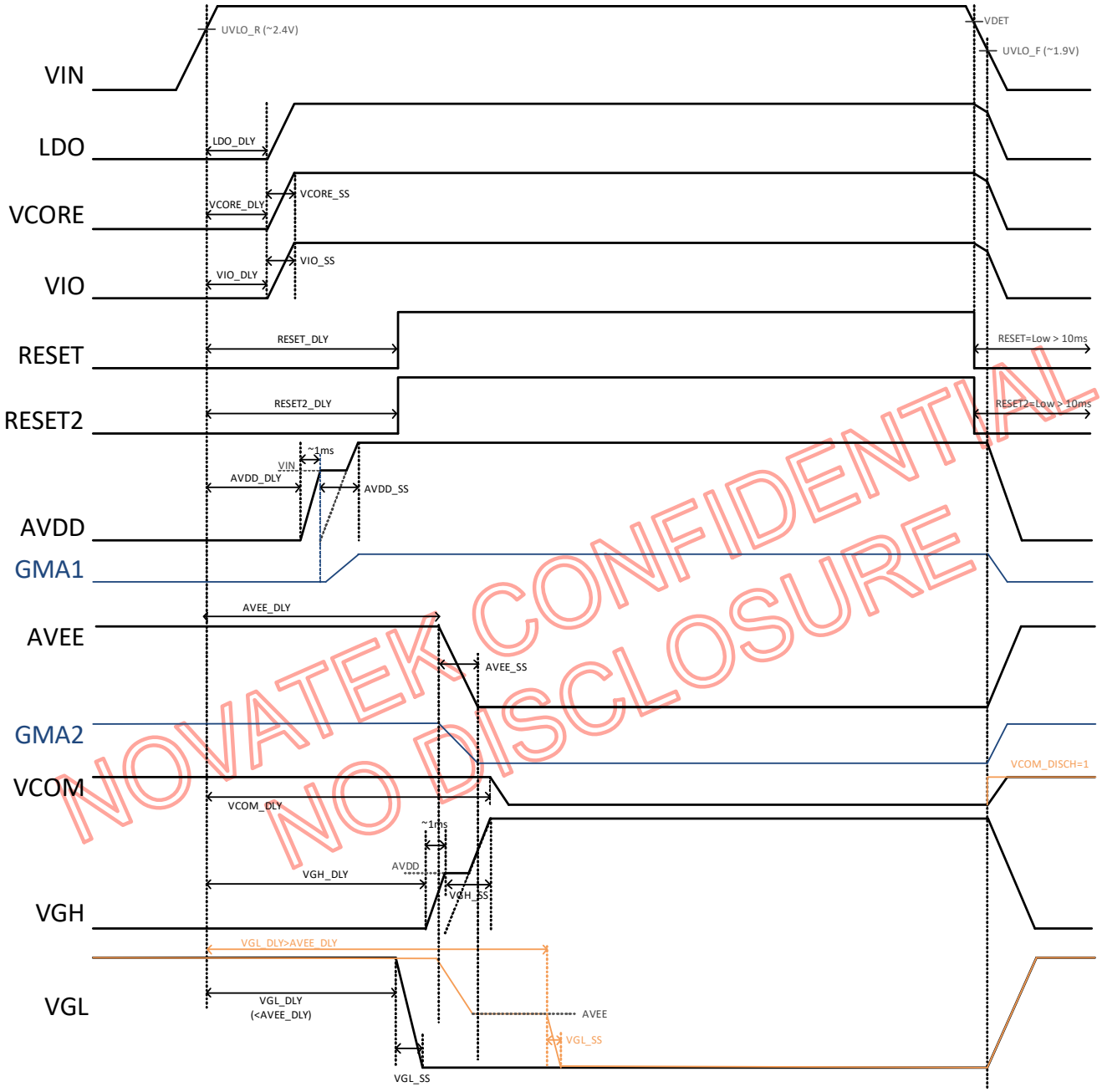
Power ON/OFF Sequence (SIBO VINP from AVDD)



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When SIBO VINP From AVDD, the delay time of VGH and VGL must be set after AVDD Voltage was ready.

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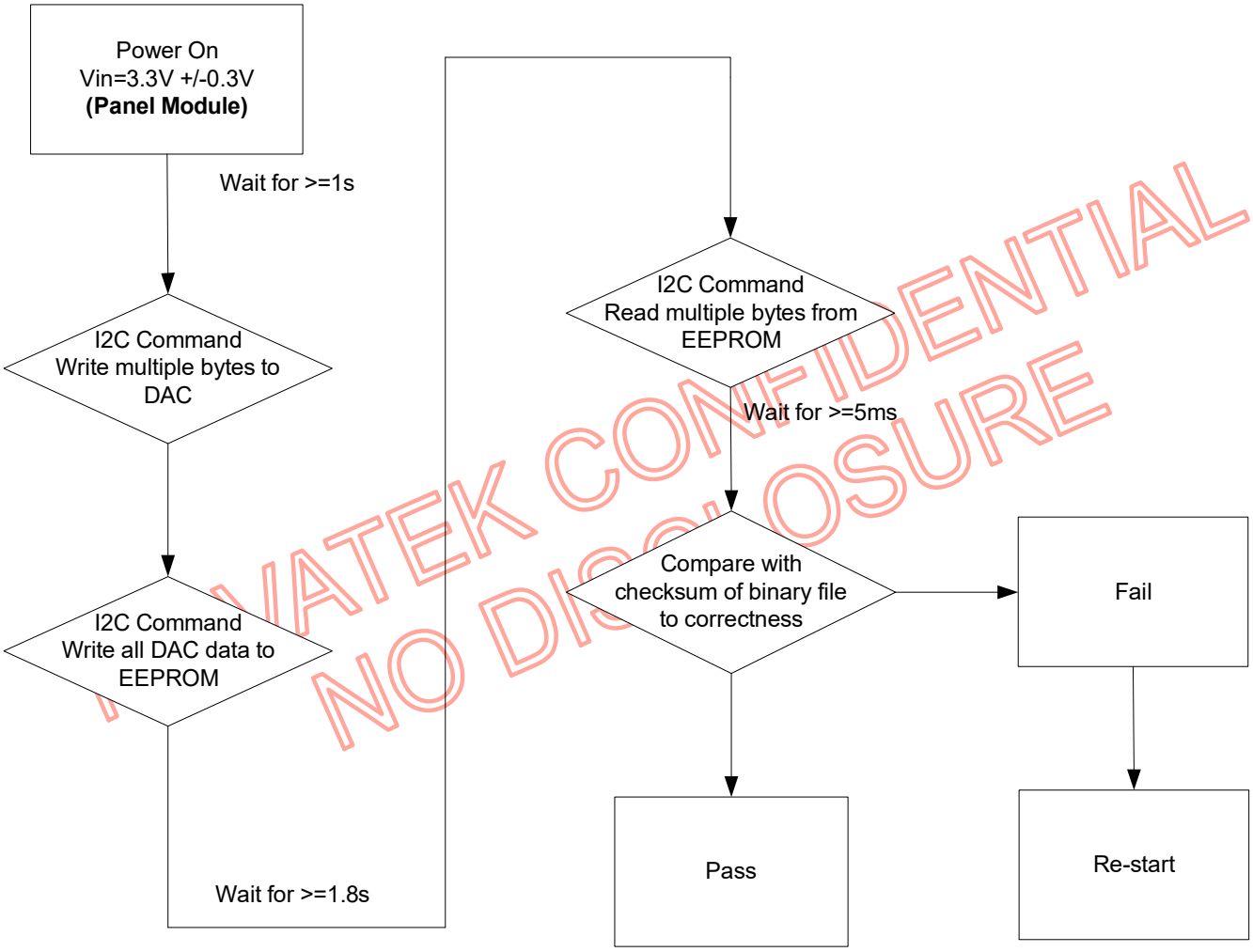
Multiple Read/Write Procedure for Panel Module: (版本1. No Write protect)

(Method 1)

Multiple Write



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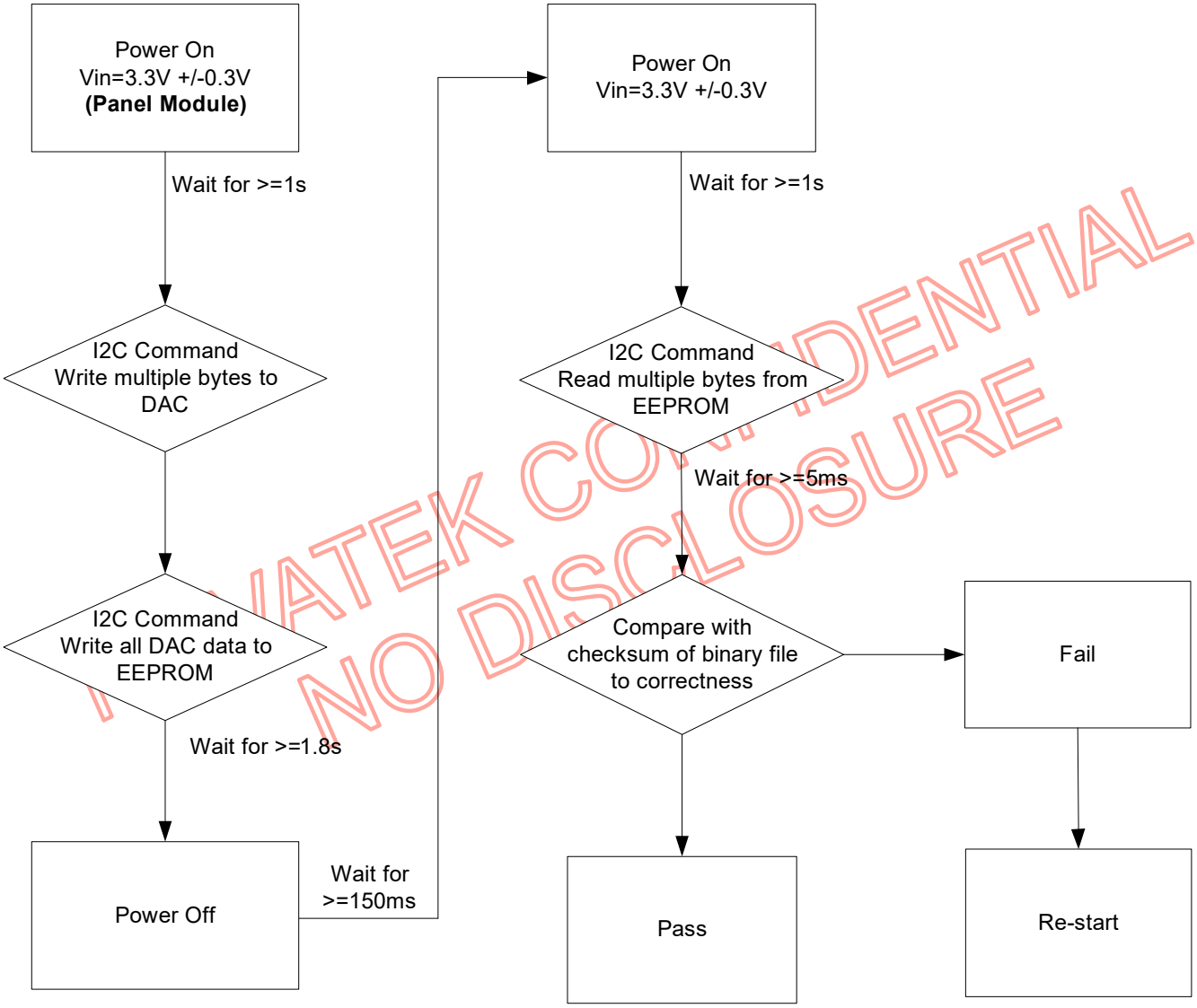
Multiple Read/Write Procedure for Panel Module: (版本1. No Write protect)

(Method 2 : Re-power on)

Multiple Write



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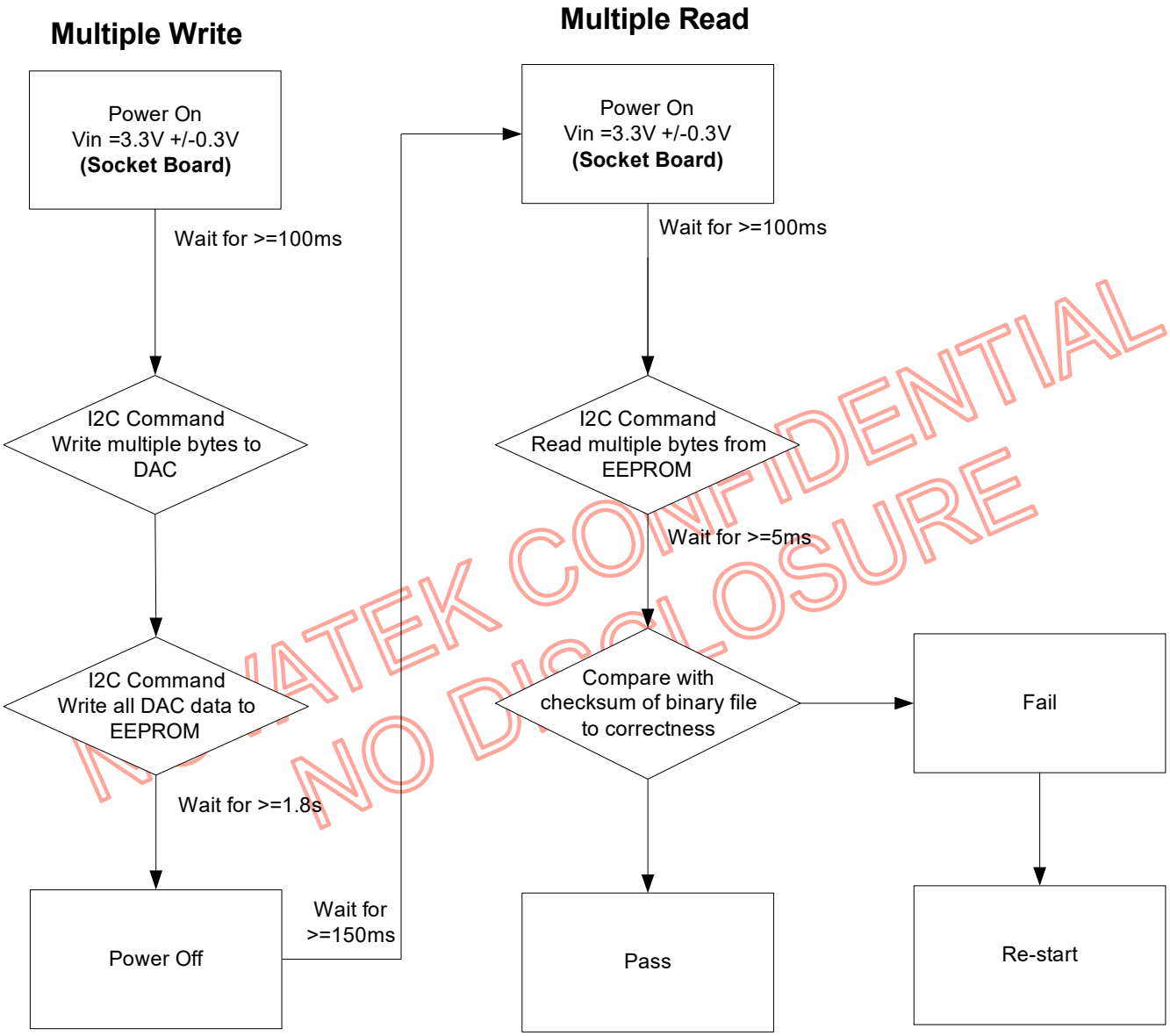
Multiple Read/Write Procedure for Single Chip: (版本 1. No Write protect)



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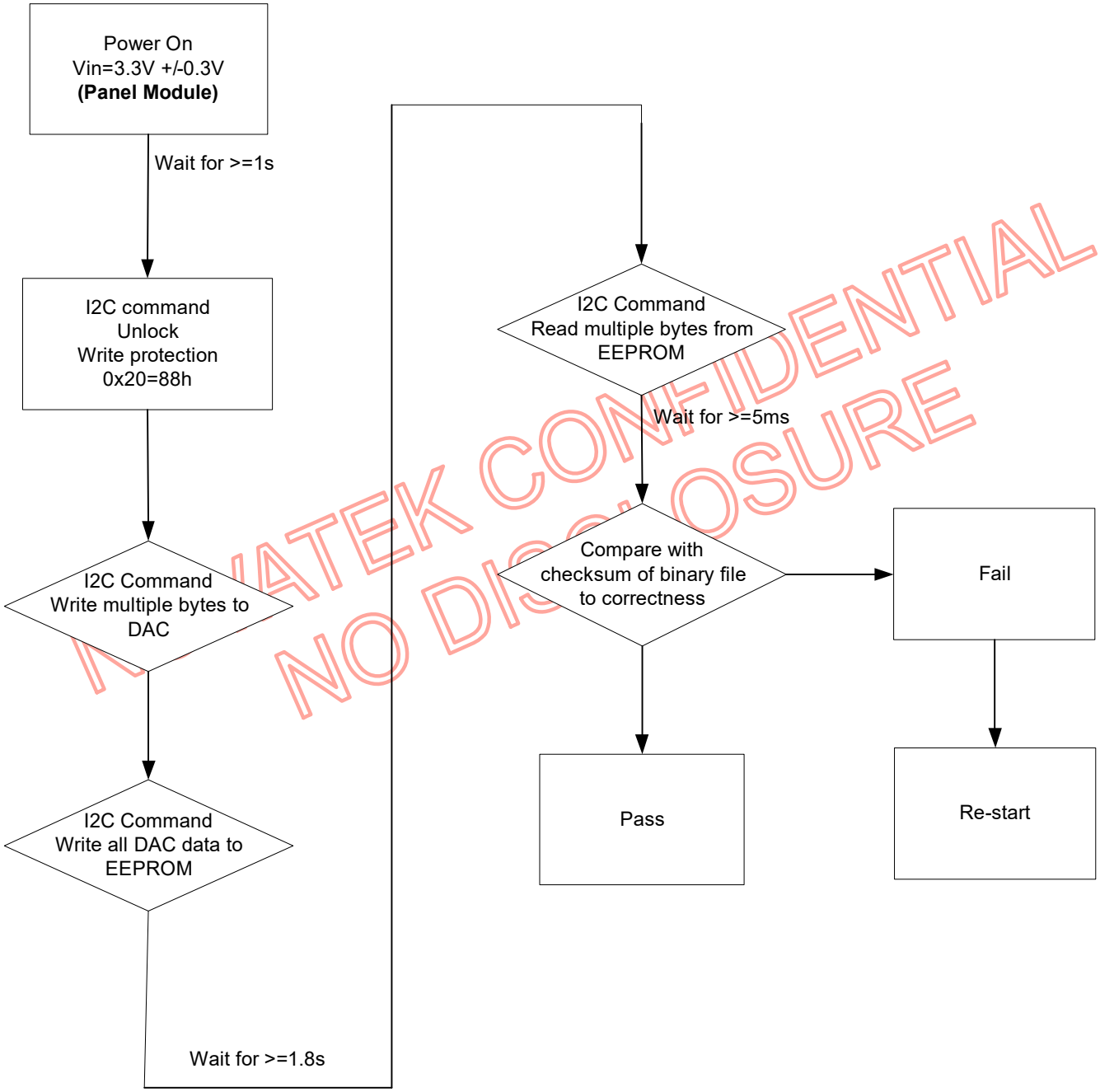
Multiple Read/Write Procedure for Panel Module: (版本 2.有 Write Protect) (Method 1)

Multiple Write



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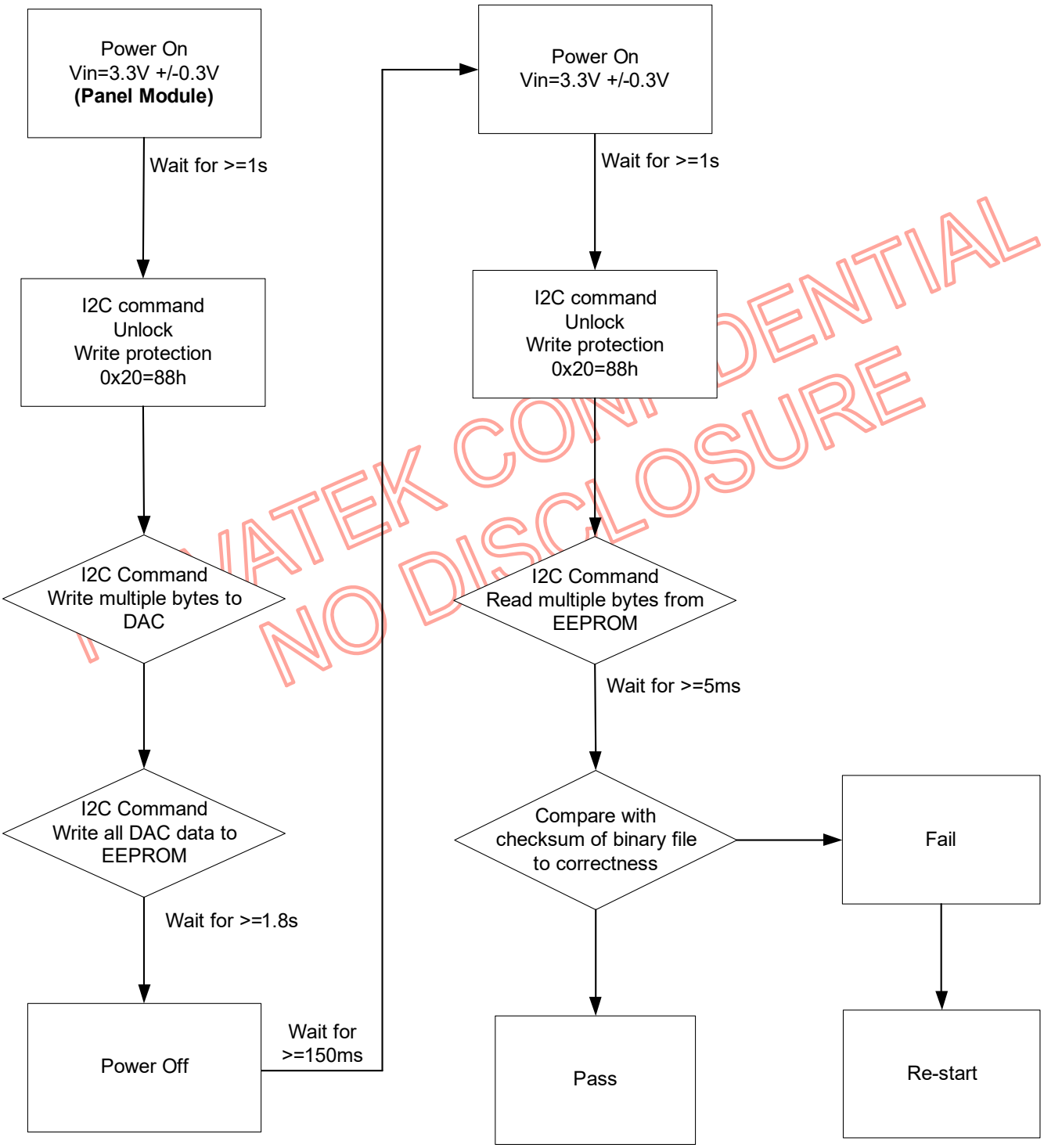
Multiple Read/Write Procedure for Panel Module: (版本 2.有 Write Protect)

(Method 2 : Re-power on)

Multiple Write



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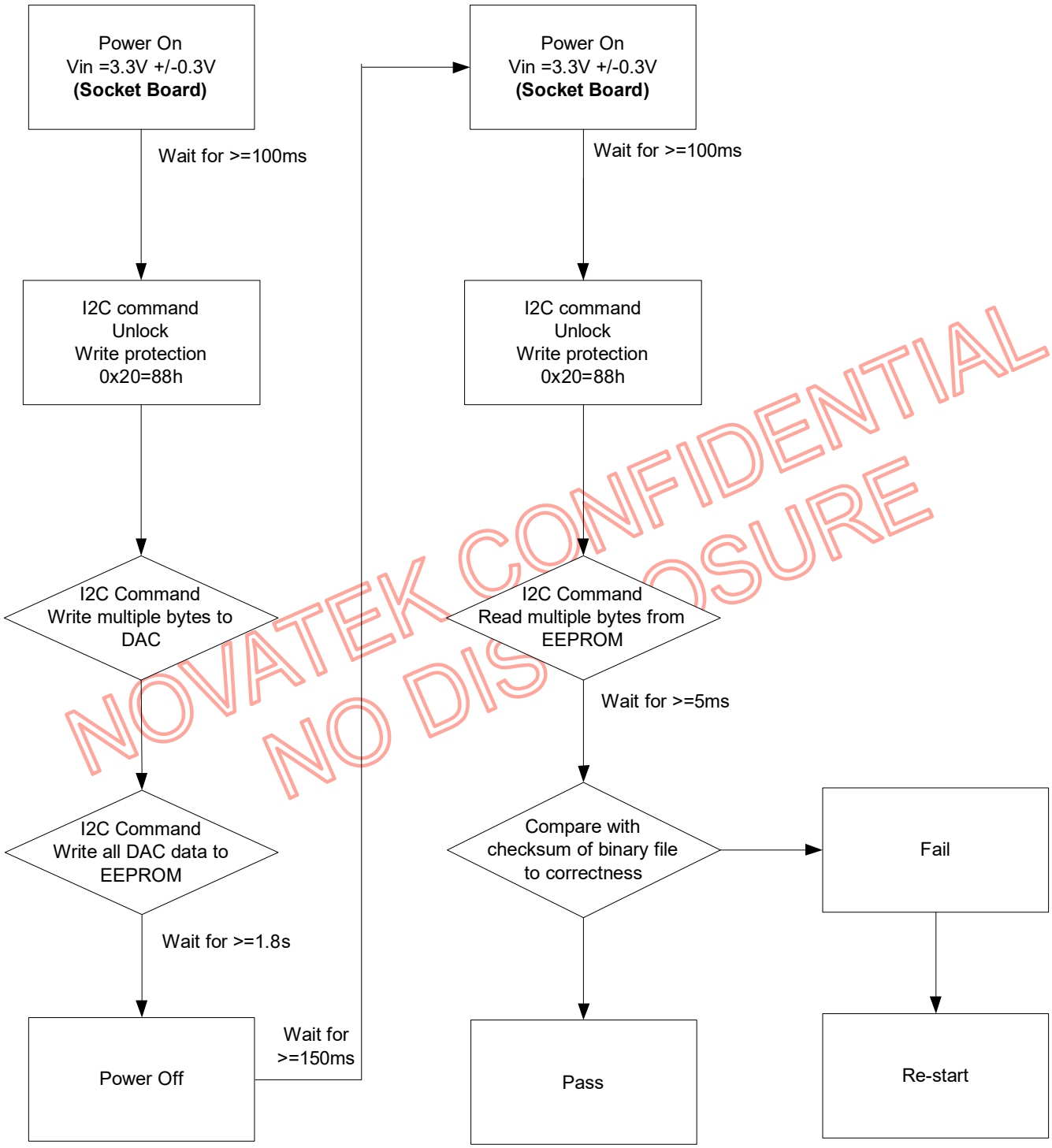
Multiple Read/Write Procedure for Single Chip: (版本 2.有 Write Protect)



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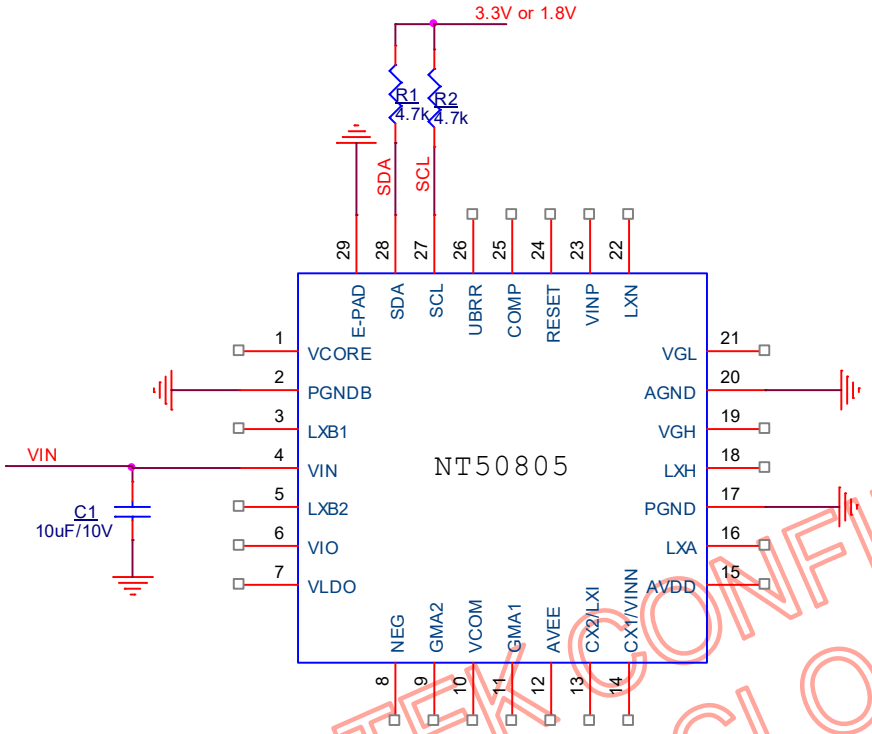
NT50805 Unit Coding Circuit for Single Chip



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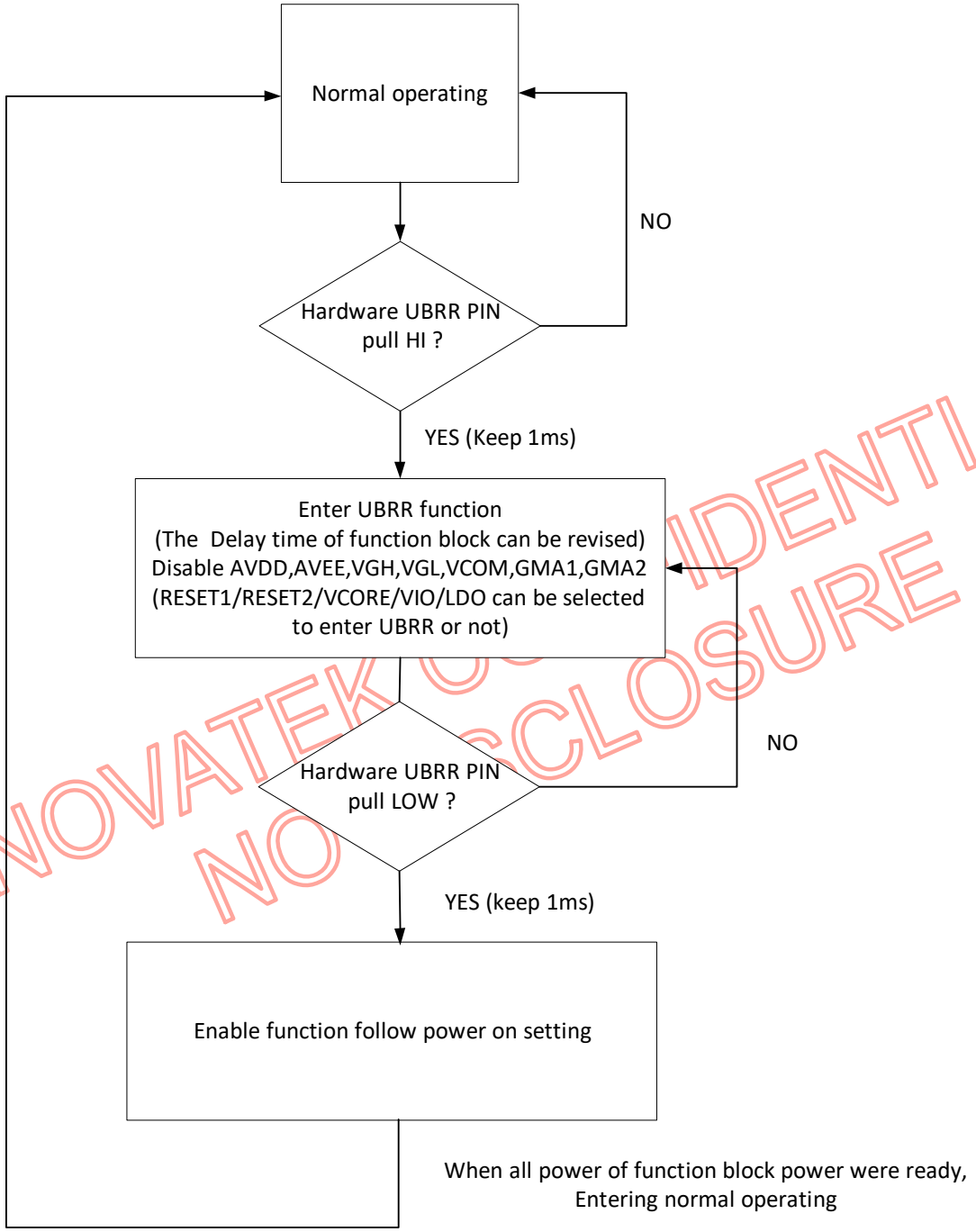
Hardware UBRR function



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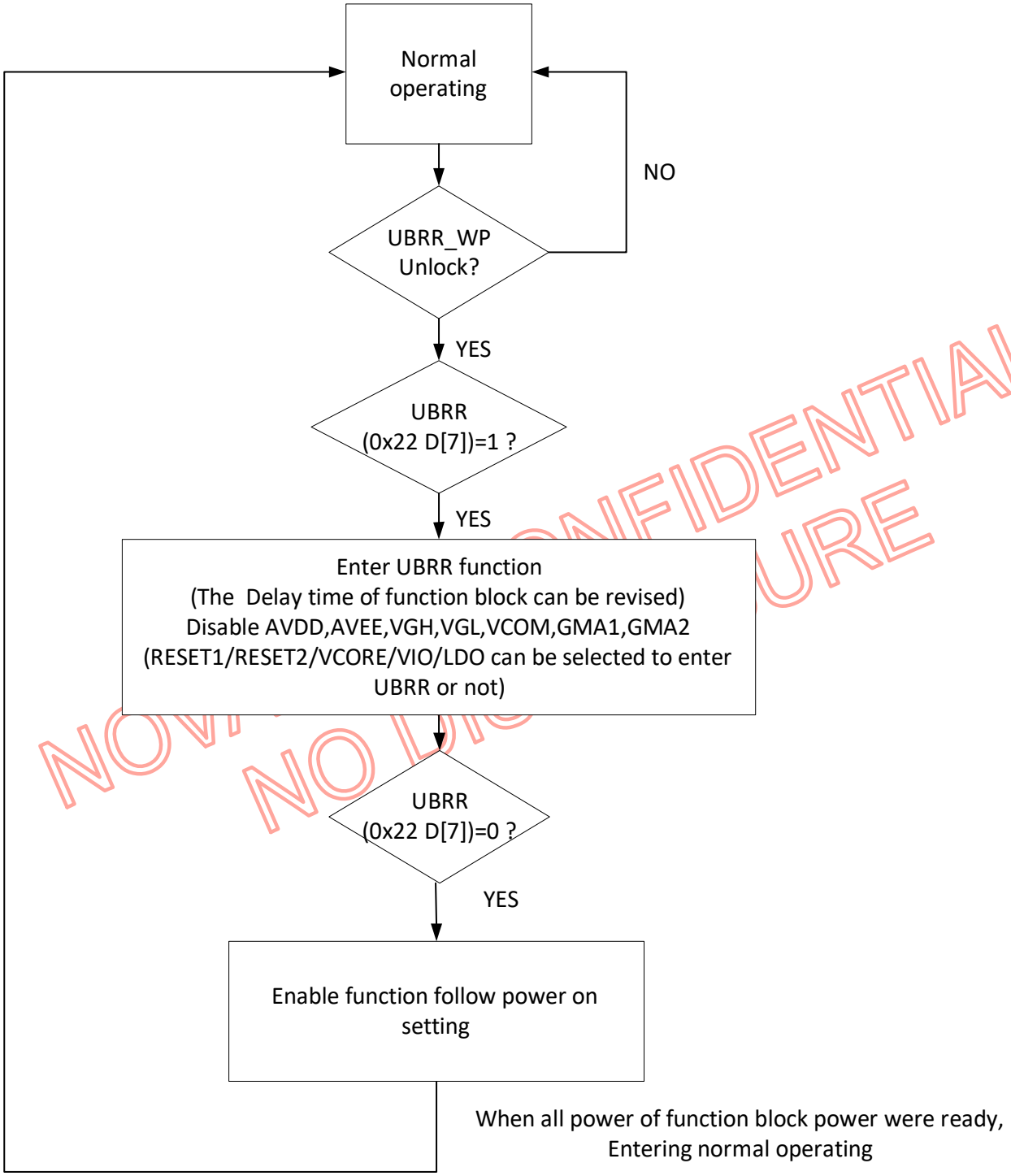
Software UBRR function



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Layout Guide

In DC to DC converters, layout consideration is always very important to the performance. With improper layout, the converter will suffer from noise problems or the loop instability. For this reason, here are several basic guidelines which are highly recommended to obey as following described:

1) Input capacitors, output capacitors and inductors must be placed as close as possible to the IC.

2) The trace between switching node, such as LX pins, and inductor is wide, short and direct.

3) No trace is allowed to go through the bottom side of inductors.

4) It is not recommended that any trace is overlapped with switching trace in different layers for better noise immunity. If it is necessary, the overlapped area must be as small as possible.

5) It is not recommended that any trace is parallel with switching trace without space or ground path between them.

6) In the PCB layout, analog ground (AGND) and power ground (PGND) are separated. AGND and PGND are connected together at the input power terminal.

7) Maximize the ground plane connected to ground pin and add via holes to the ground plane in other PCB layers.

8) Connect capacitors to solid ground directly to get the good performance.

9) Place some via holes under the IC to spread heat easily.

10) To prevent I*R loss, the trace from VIN bus to IC application circuit must be short and wide.

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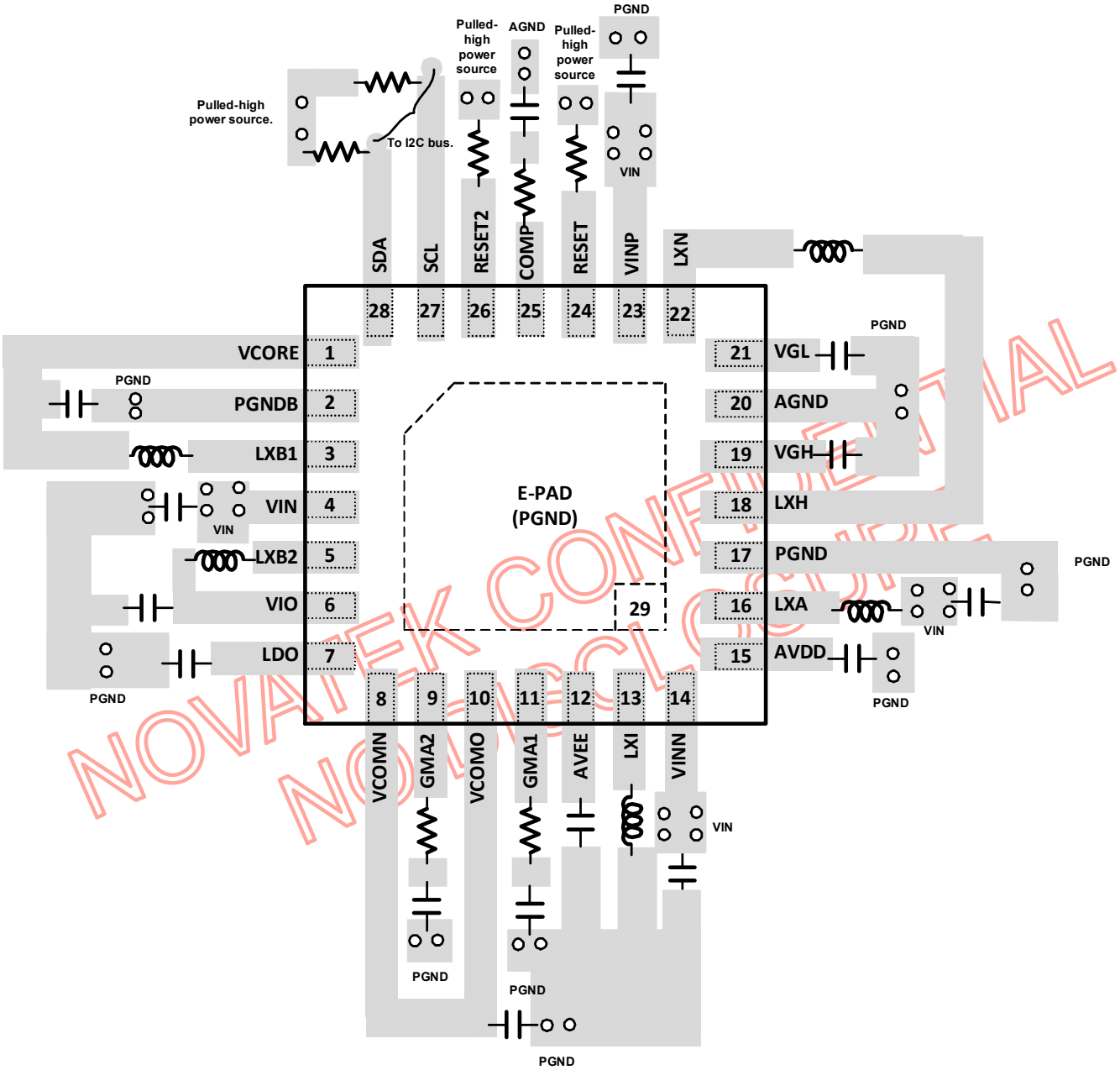
For PIN26=RESET2



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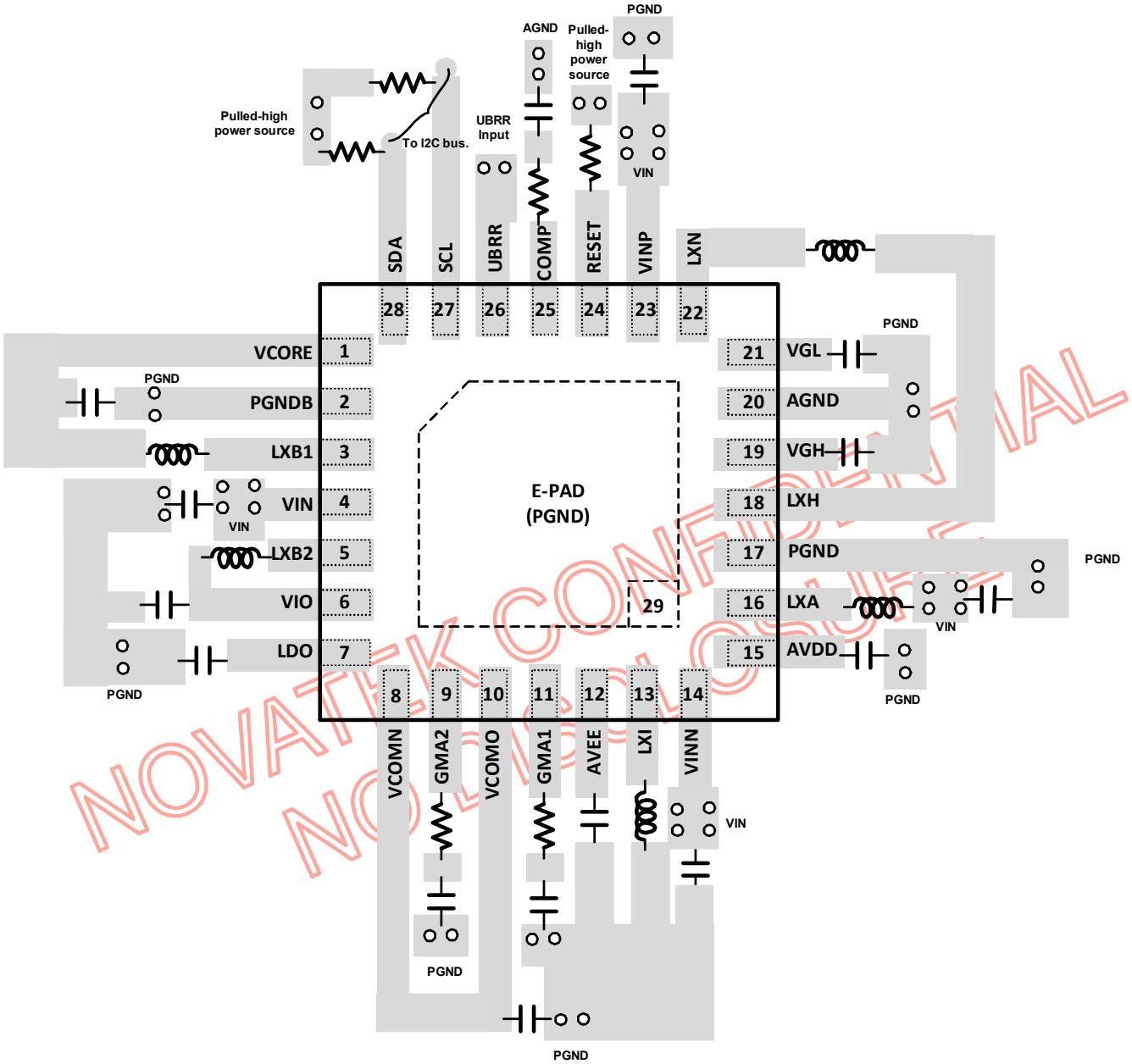
For PIN26=UBRR



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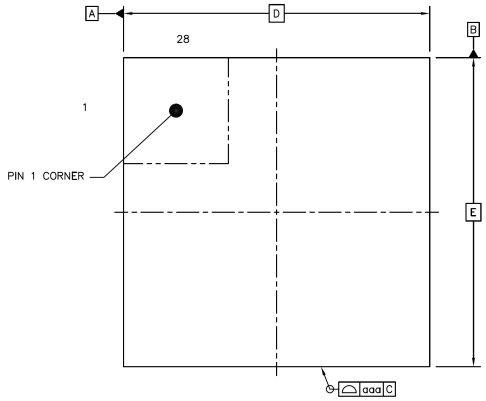
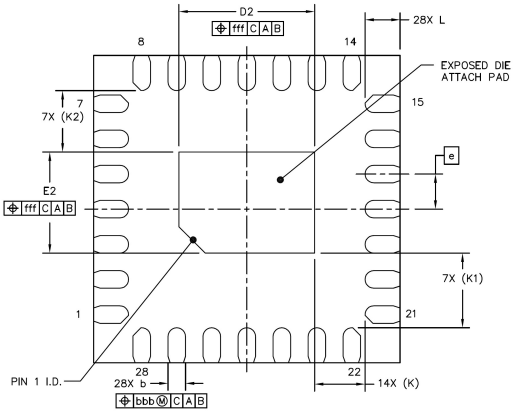
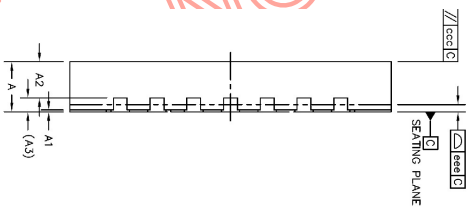
Package Information (FCQFN3.5x3.5)



Dimension in millimeters

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3.5 BSC		
	Y	E	3.5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	1.5	1.55	1.6
	Y	E2	1.1	1.15	1.2
LEAD LENGTH		L	0.35	0.4	0.45
LEAD TIP TO EXPOSED PAD EDGE		K	0.575 REF		
		K1	0.85 REF		
		K2	0.7 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
EXPOSED PAD OFFSET		fff	0.1		





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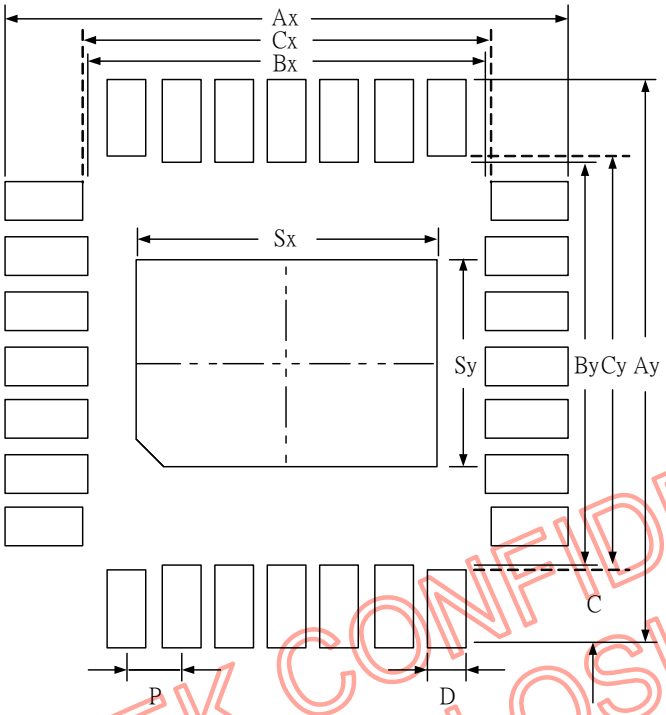
Footprint Information (FCQFN3.5x3.5)



Dimension in millimeters

Package	Number of Pin	Tolerance											Tolerance
		P	Ax	Ay	Bx	By	Cx	Cy	C	D	Sx	Sy	
FCQFN 3.5x3.5-28L	28	0.40	4.30	4.30	2.70	2.70	2.90	2.90	0.8	0.20	1.55	1.15	±0.050

Note 1: Rounded finger pads are recommended to prevent solder bridging.

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Important Notice

NT50805 is a product that is not specifically designed and marketed, and shall not be directly and/or knowingly sold or used as to be incorporated into, any of the following products:

(i) military products or proliferation application (including but not limited to missiles, nuclear, chemical and biological weapons); or
(ii) commercial space products or applications that are controlled under the U.S. Munitions List (USML); or
(iii) medical appliances; and
(iv) automotive driver safety assistant system

furthermore, NT50805 shall not be directly and knowingly shipped to any country subject to "embargo" or exported to, re-exported to, transferred to, or used by any restricted entity, including but not limited to those listed on the U.S. Department of Commerce Entity List, under the U.S. laws and or its applicable regulations (e.g., the U.S. Export Administration Regulations) in effect from time to time.

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